

PEGATRON CONFIDENTIAL

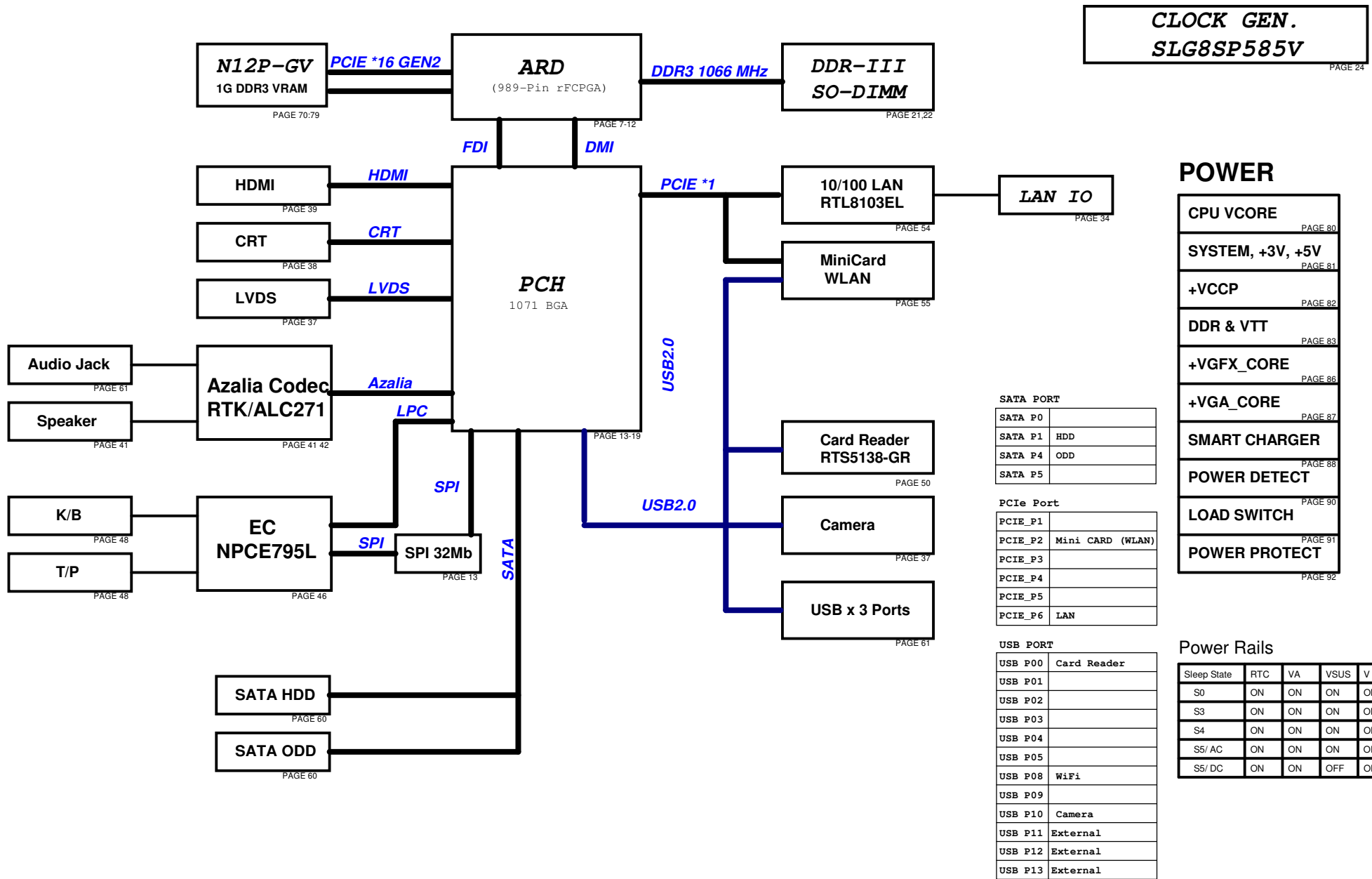
MODEL NAME :

PCB NO :

69- P/N :

AIC70 Schematic  
Intel Arrandale rPGA-989  
PCH BGA 1071  
2011-05-04  
REV : R2.0

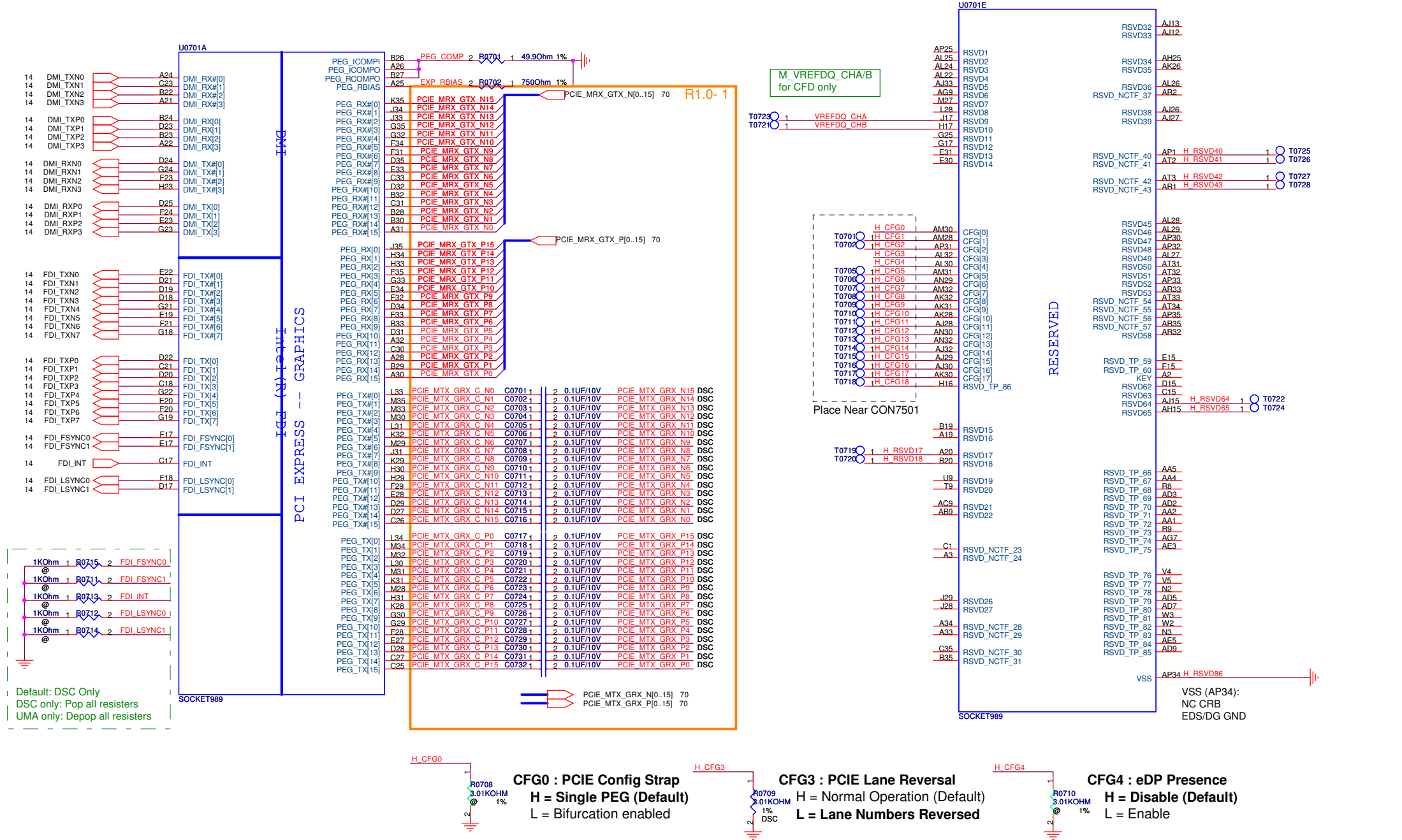
# AIC70 BLOCK DIAGRAM

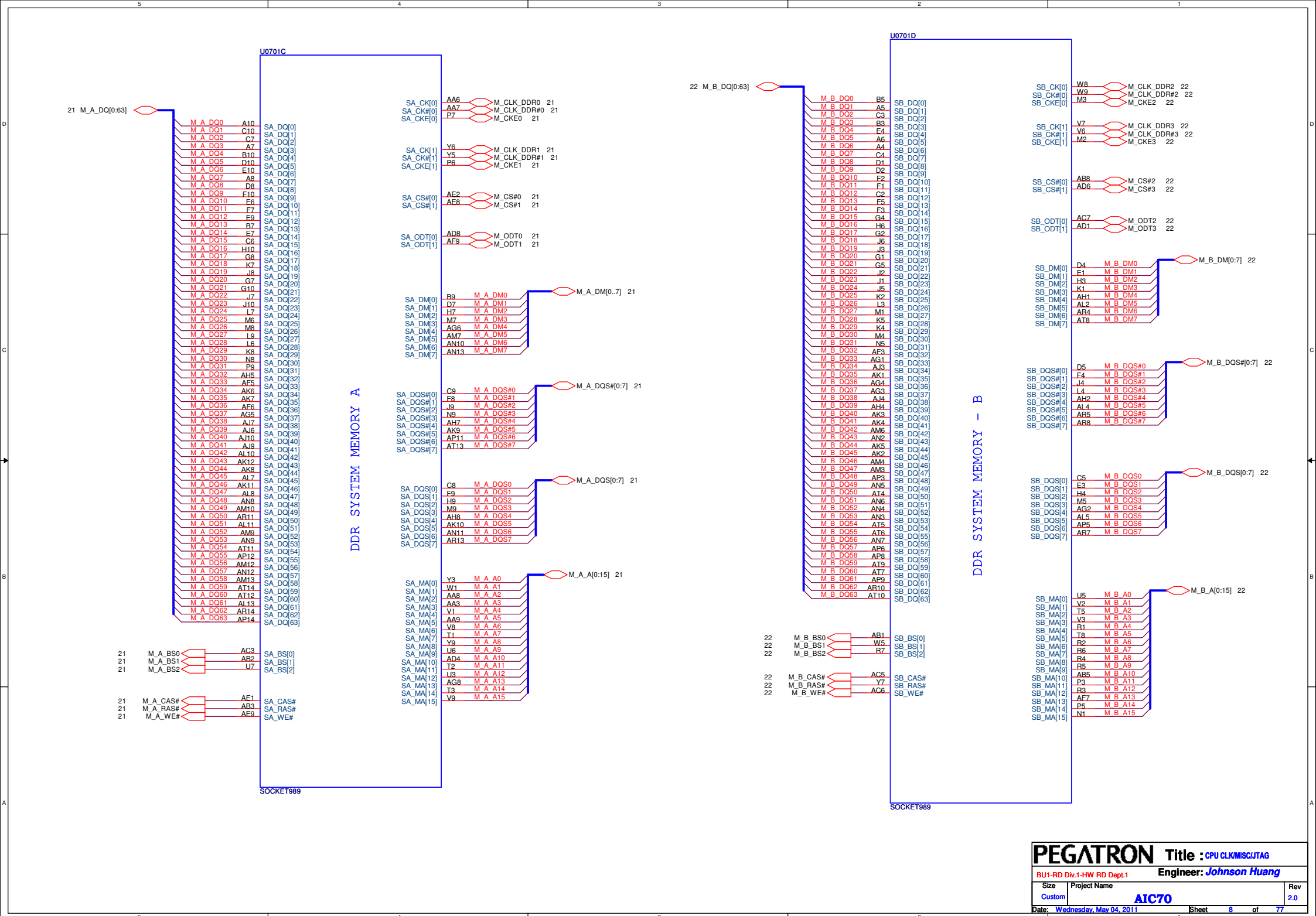


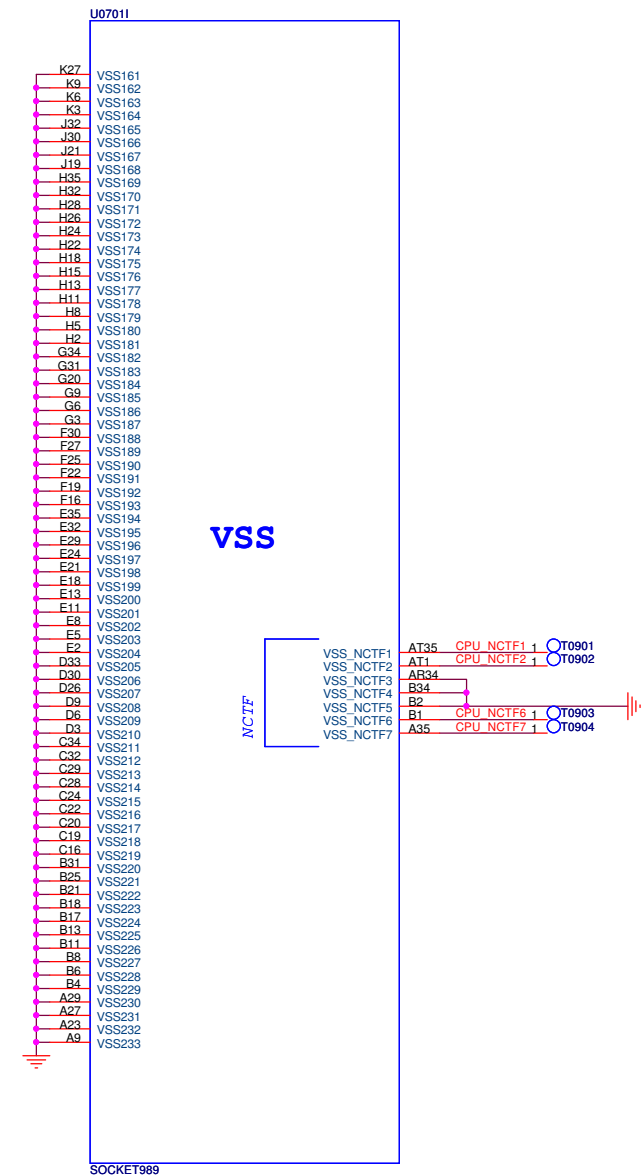
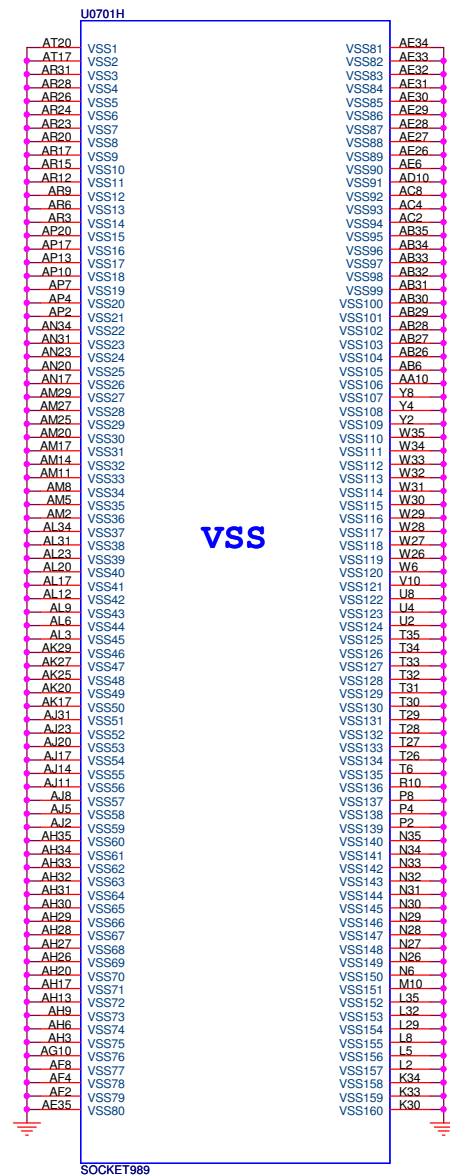
SCHEMATIC INDEX V1.2

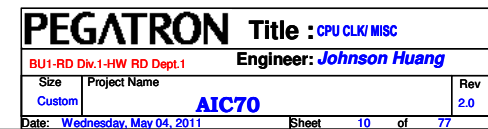
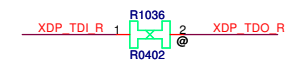
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50	CARD READER	
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95	EE History	
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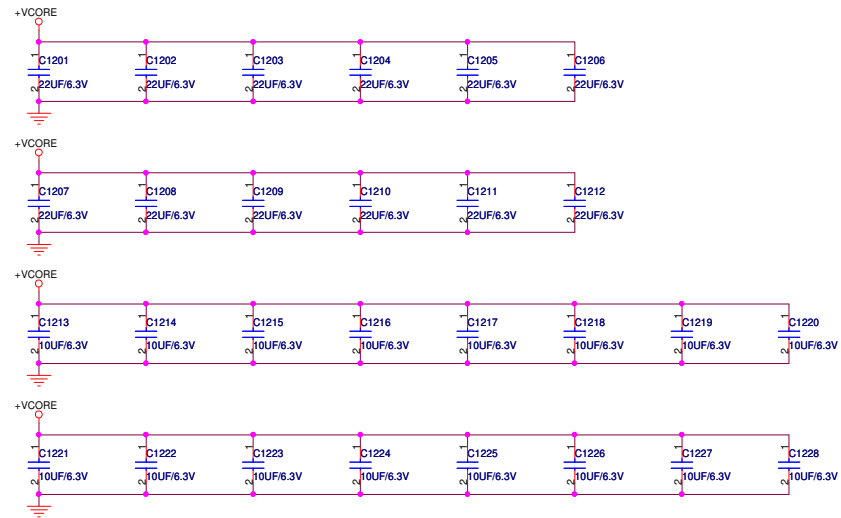




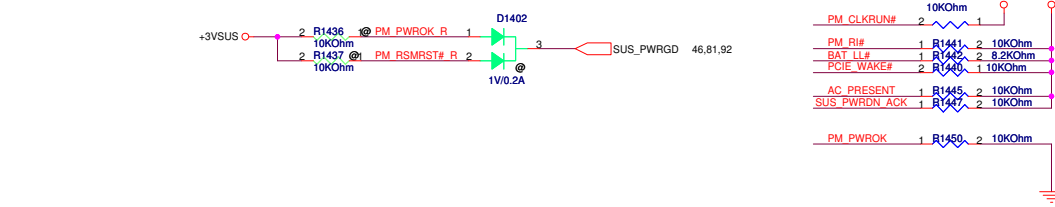
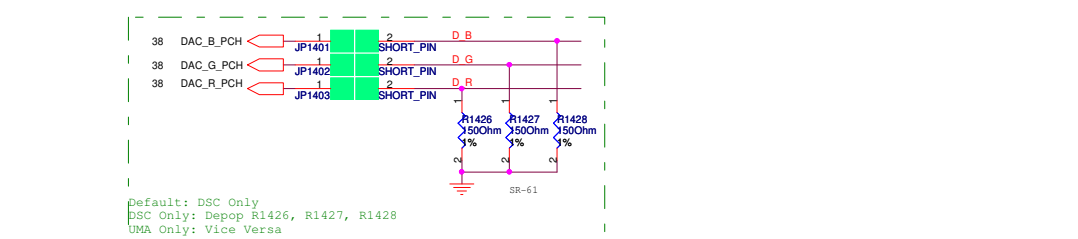
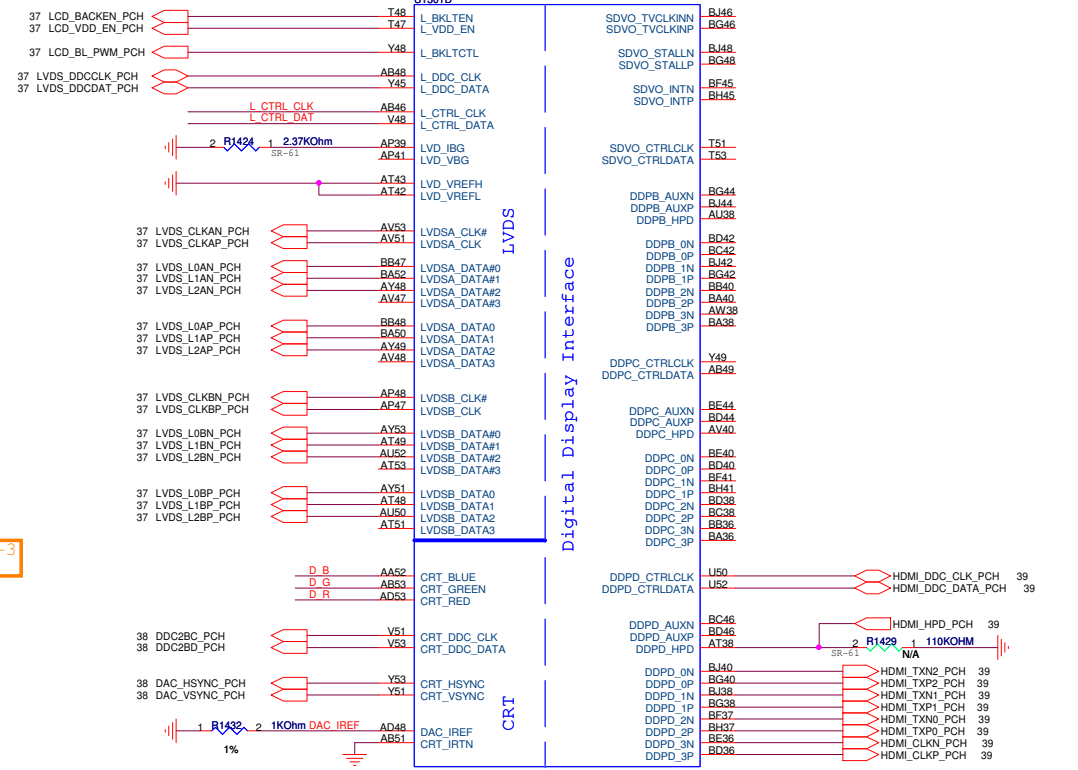
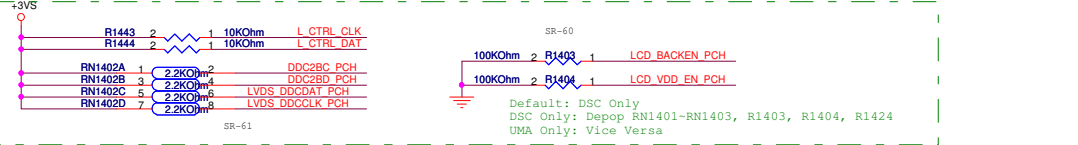
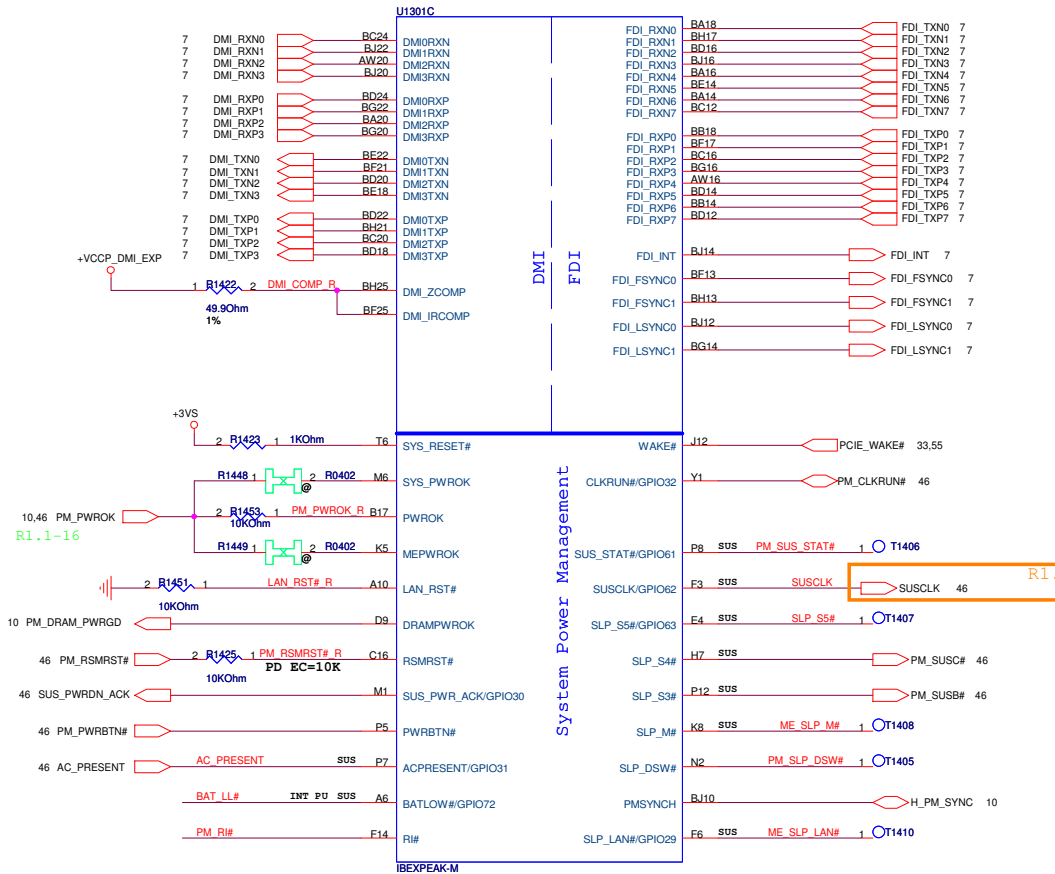


Decoupling guide from INTEL

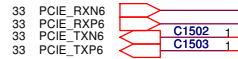
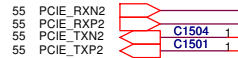
VCORE	10uF	x 16pcs
	22uF	x 12pcs



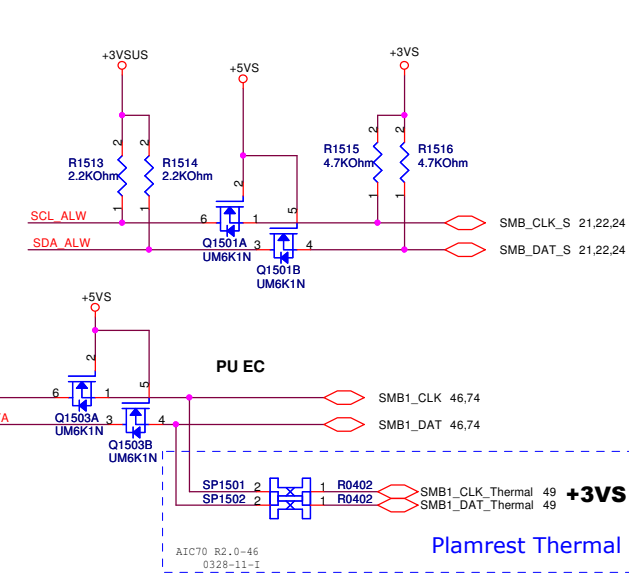
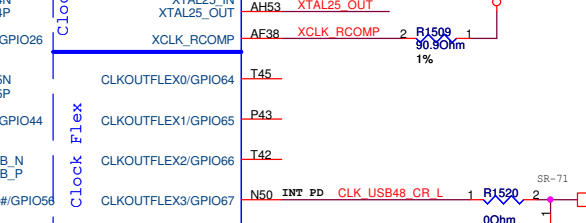
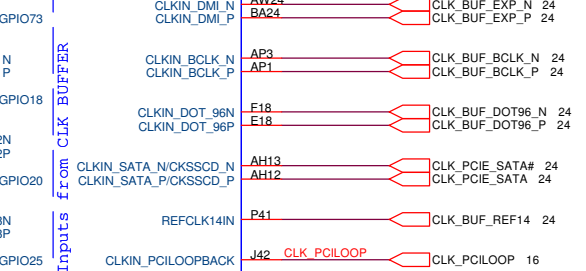
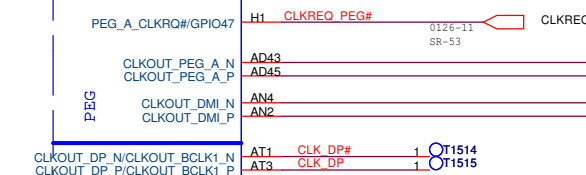
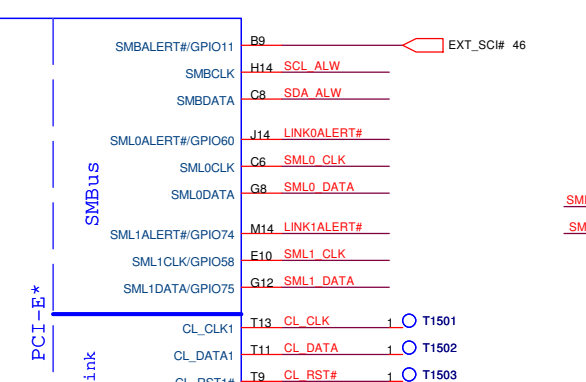
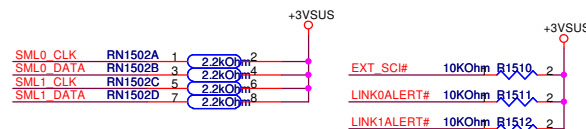
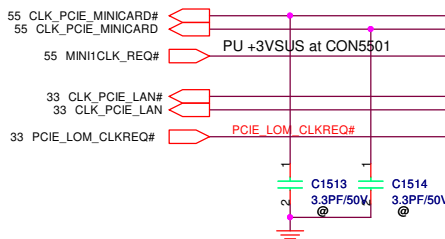
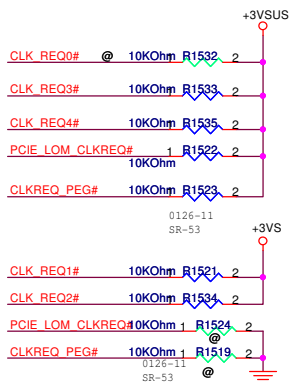




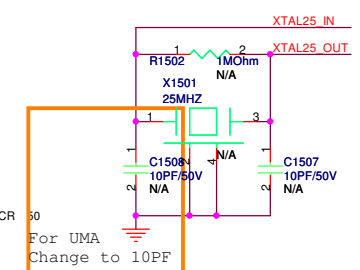
PCIE 1	
PCIE 2	Mini CARD (WLAN)
PCIE 3	
PCIE 4	
PCIE 5	
PCIE 6	LAN

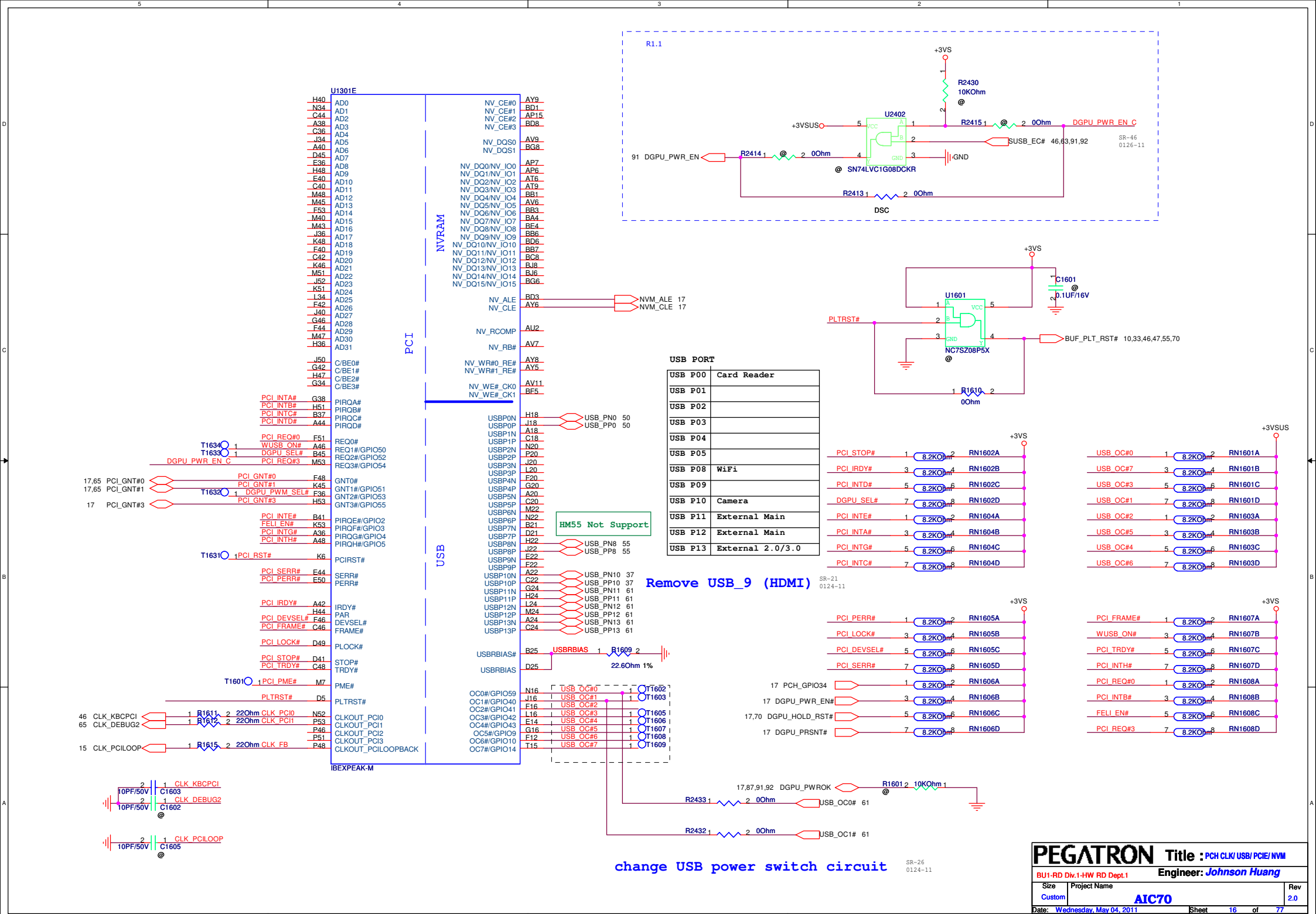


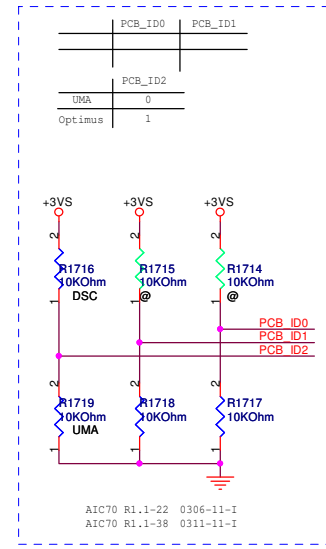
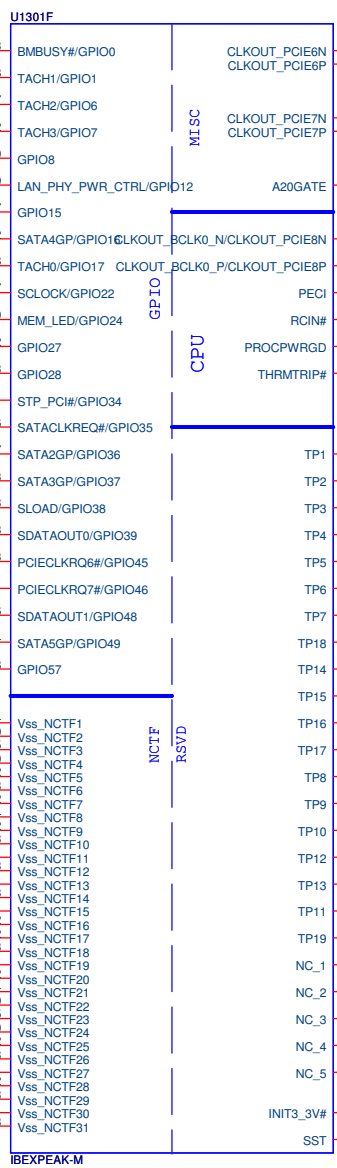
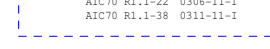
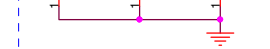
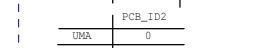
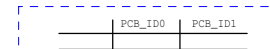
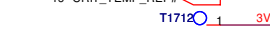
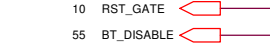
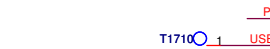
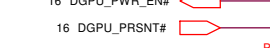
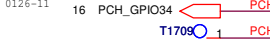
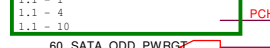
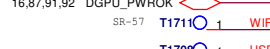
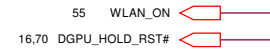
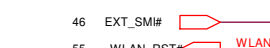
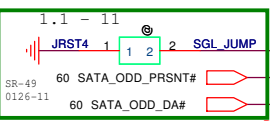
HM55 Not Support



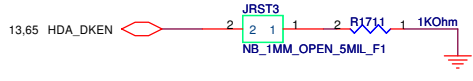
Damping CPU Side







HDA\_DKEN : Flash Descriptor Security Override  
H = Disabled (Default)  
L = Enabled  
Note : Rising edge of PWROK



NOTE:  
Assert the HDA\_DKEN will halt and disable Intel ME.  
This is a debug mode and must not asserted after manufacturing/debug.

PCH\_SPI1 : iTPM STRAP  
H : Enable iTPM  
L : Disable iTPM (Default)  
Description Only.  
No PU Reserved

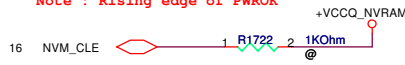
PCI\_GNT#3 : A16 swap override  
Strap/Top-Block Swap Override jumper  
H : Default  
L : A16 swap override/Top-Block Swap  
Override enabled

Note : Rising edge of PWROK



NVM\_CLE : DMI Termination Voltage  
H : Set to Vcc  
L : Set to Vss

Note : Rising edge of PWROK



GPIO15/ WLAN\_ON :  
H = Intel ME Crypto Transport Layer Security (TLS)  
cipher suite with confidentiality  
L = Intel ME Crypto Transport Layer Security (TLS)  
cipher suite with no confidentiality

Note : Rising edge of RSMRST# pin



PCH\_INTVRMEN : Integrated SUS 1.05V VRM Enable  
H : Integrated VRM is enabled  
L : Integrated VRM is disabled  
Note : This signal should always be pulled high



SPKR\_PCH : NO REBOOT STRAP  
H : Enable  
L : Disable (Default)

Note : Rising edge of PWROK



PCI\_GNT#1, PCI\_GNT#0 : Boot BIOS Strap

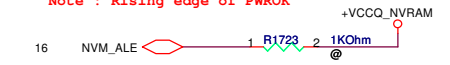
PCI_GNT#0	PCI_GNT#1	
0	0	LPC
0	1	PCI
1	1	SPI

Note : Rising edge of PWROK



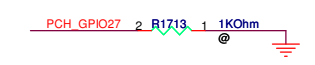
NVM\_ALE : Danbury Technology Enabled  
High--> Enable Intel Anti-Theft Technology.  
Low--> Disable Intel Anti-Theft Technology.

Note : Rising edge of PWROK



GPIO27/ USB\_SW :  
H = Enables the internal VccVRM. (Default)  
L = Disables the VccVRM.

Note : Rising edge of RSMRST# pin



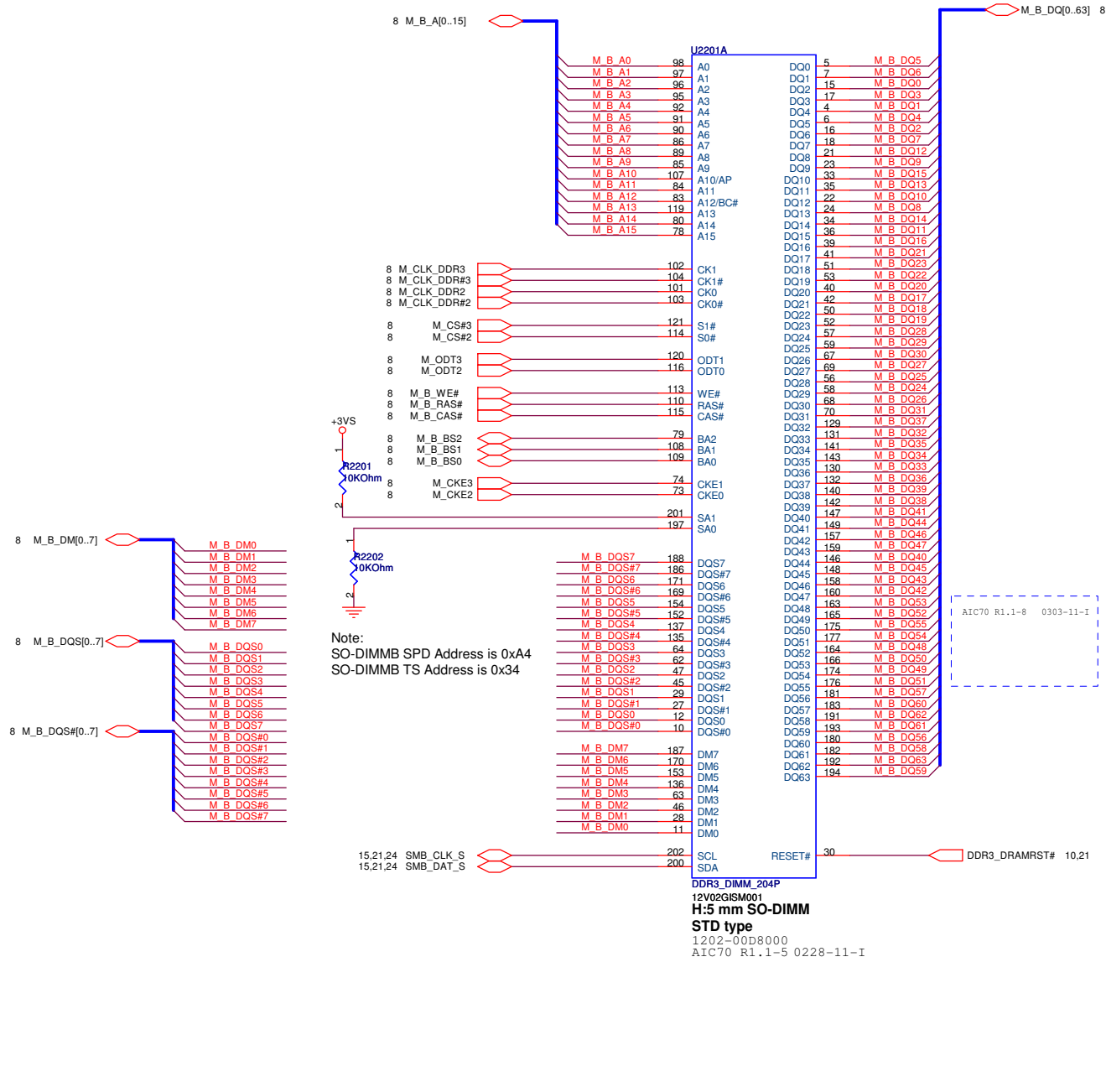


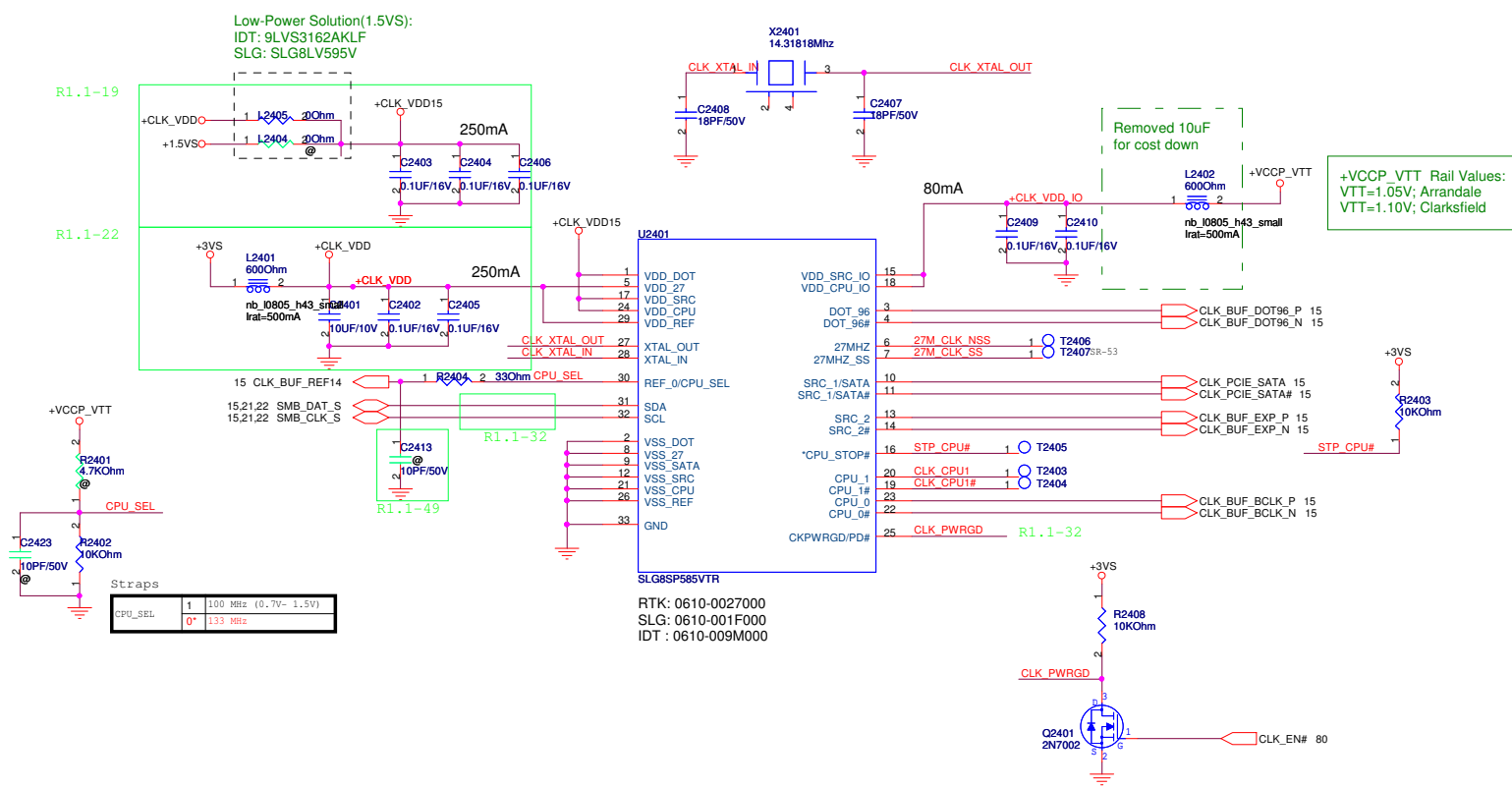




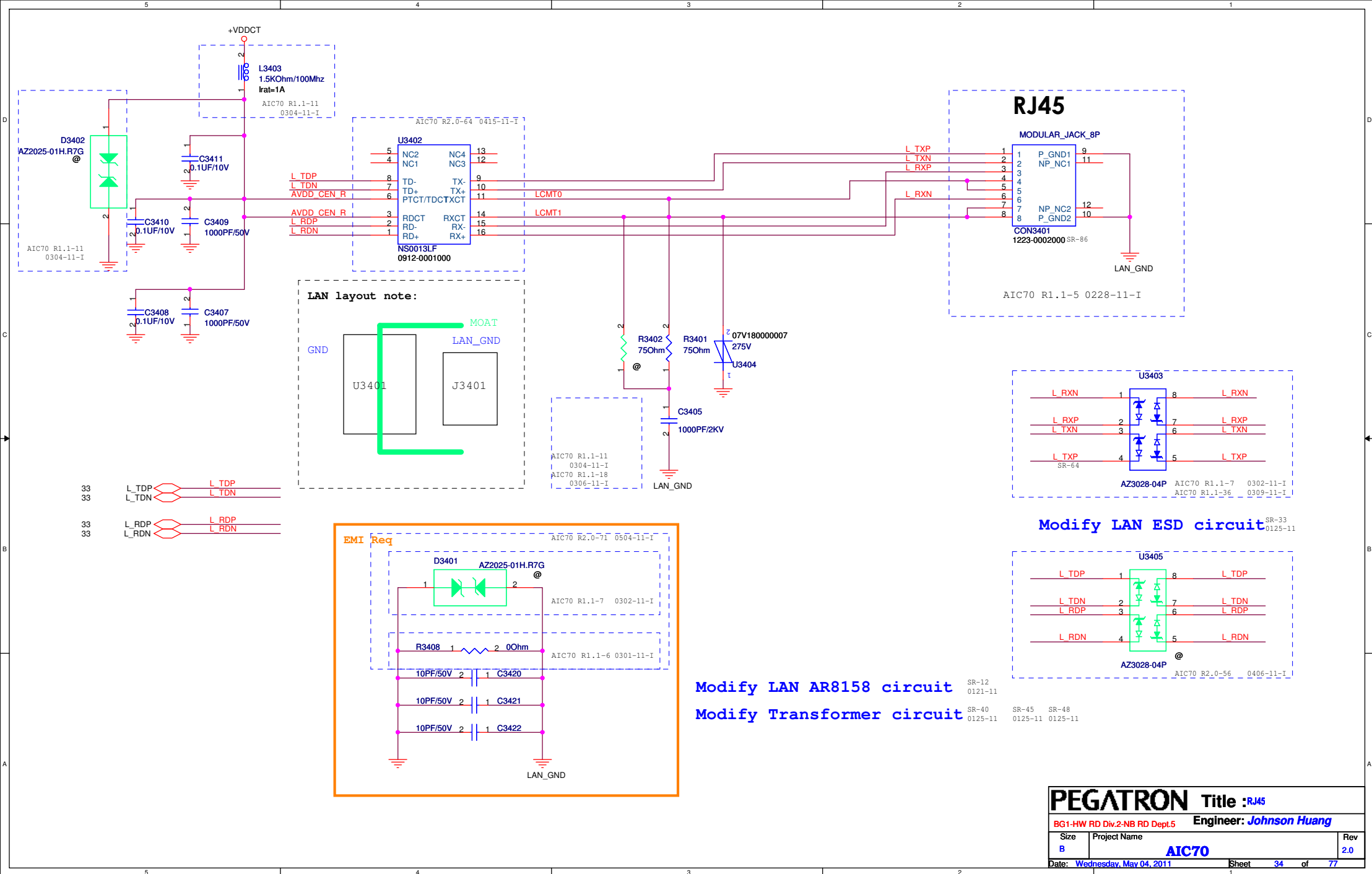




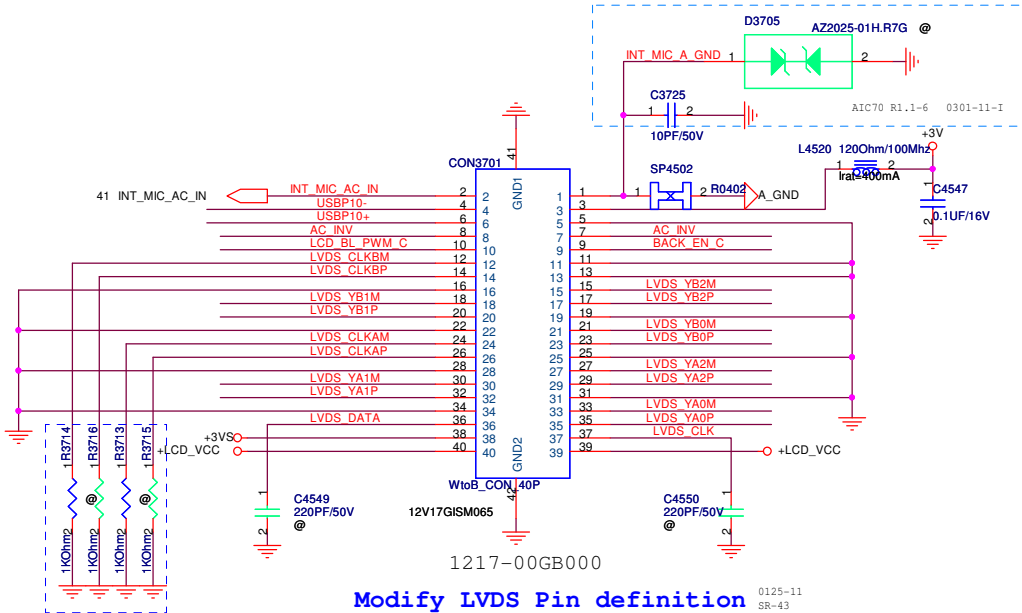




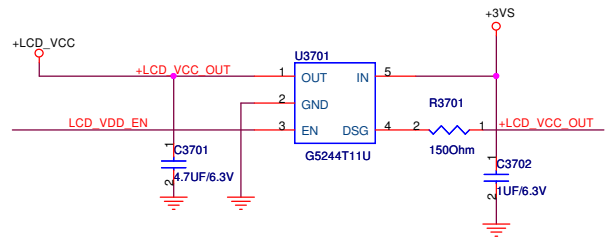
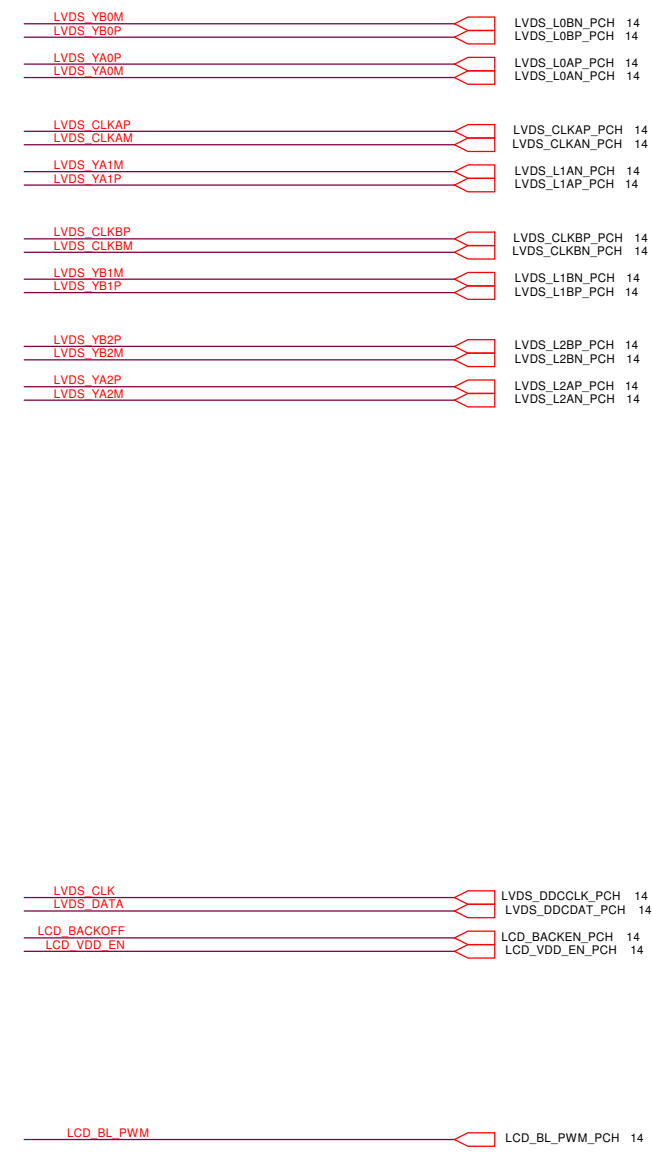
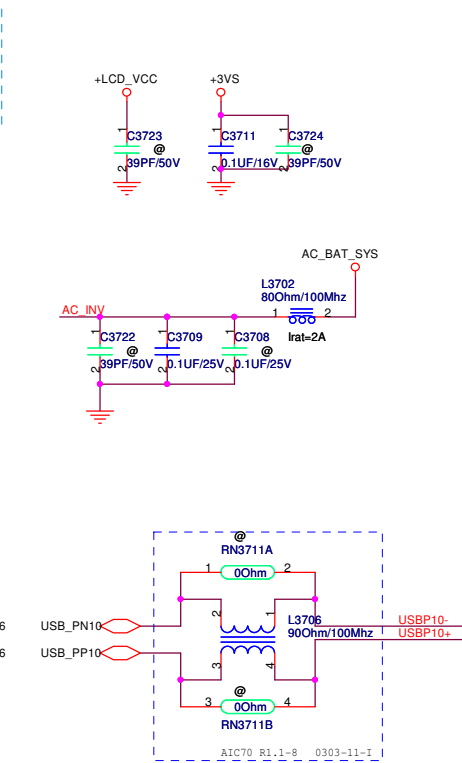
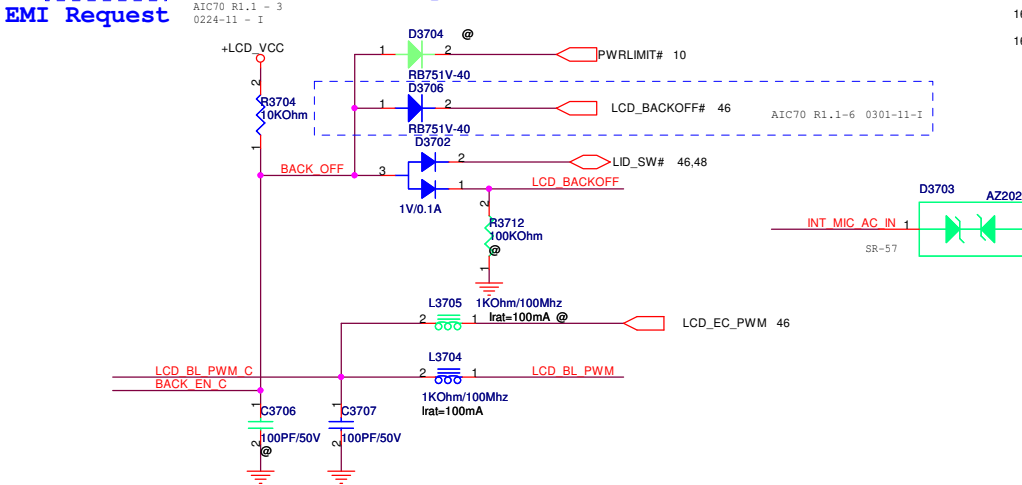


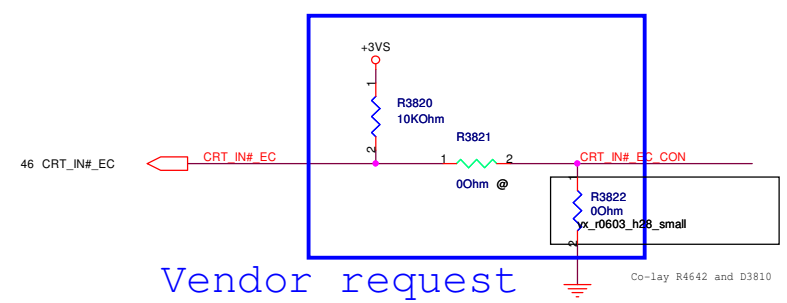
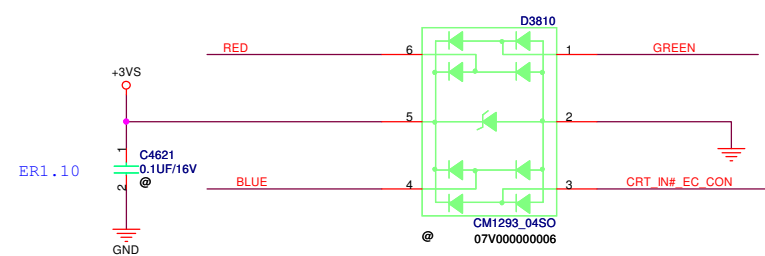
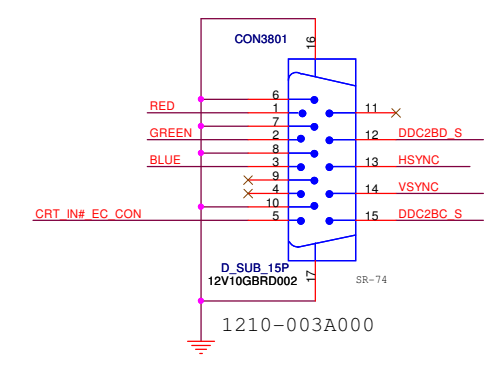
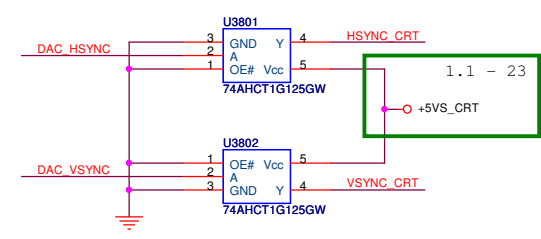
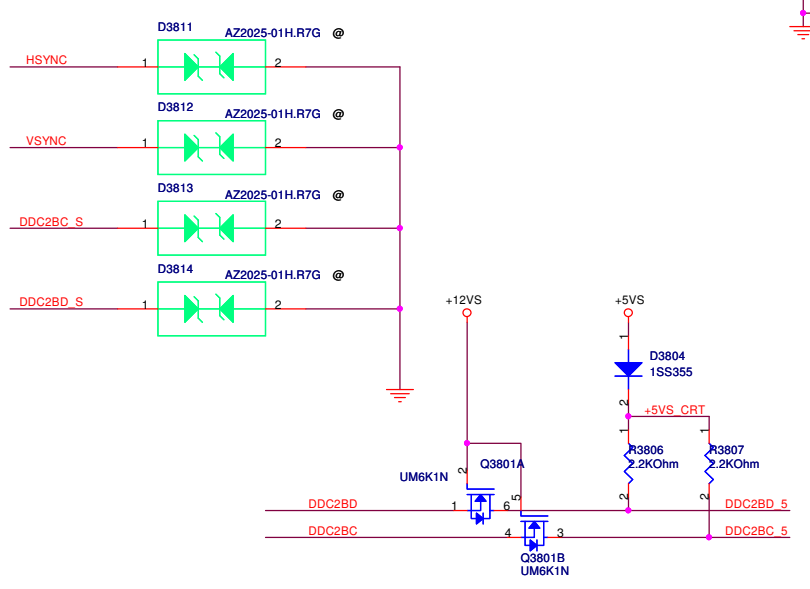
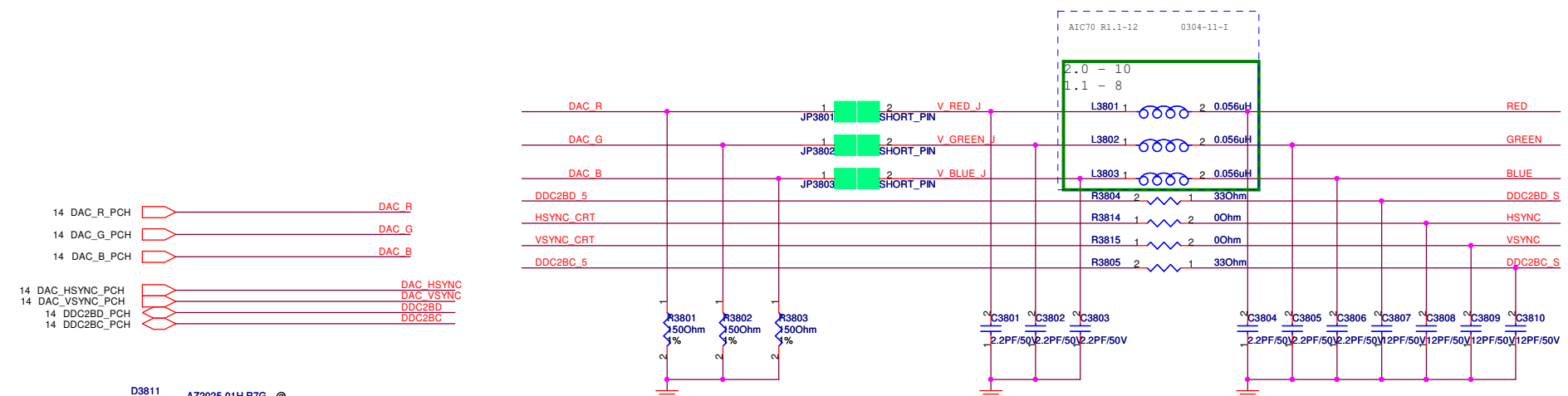


# LVDS Conn w/Camera Module & Int Mic



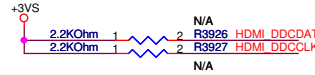
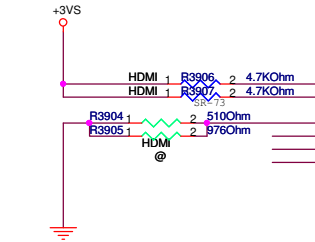
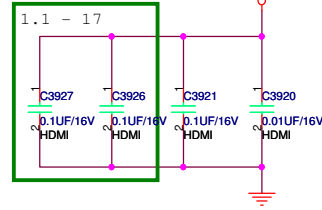
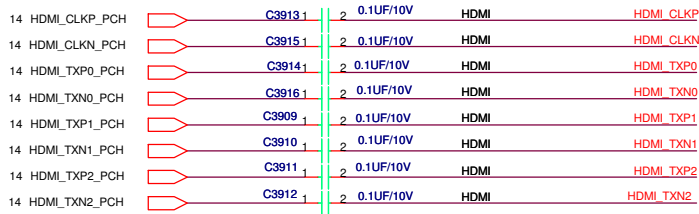
Modify LVDS Pin definition



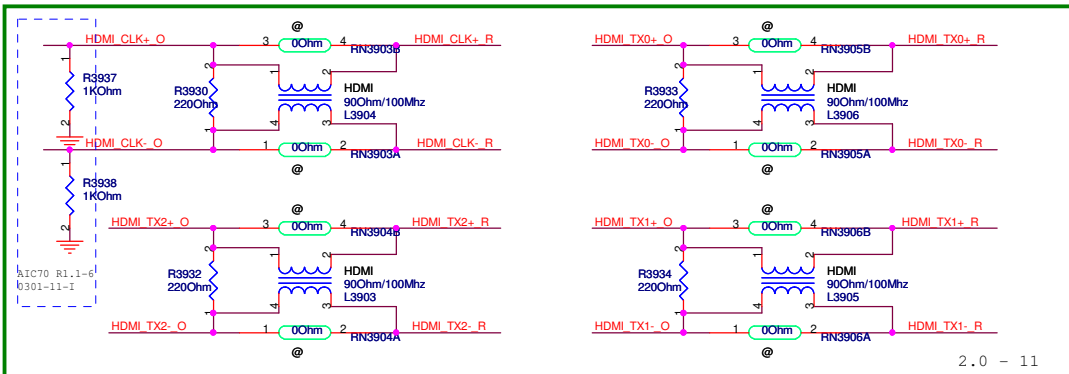


Del F3801, C3811 ADD CRT IN SR-36 0125-11

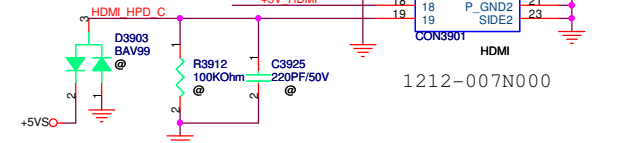
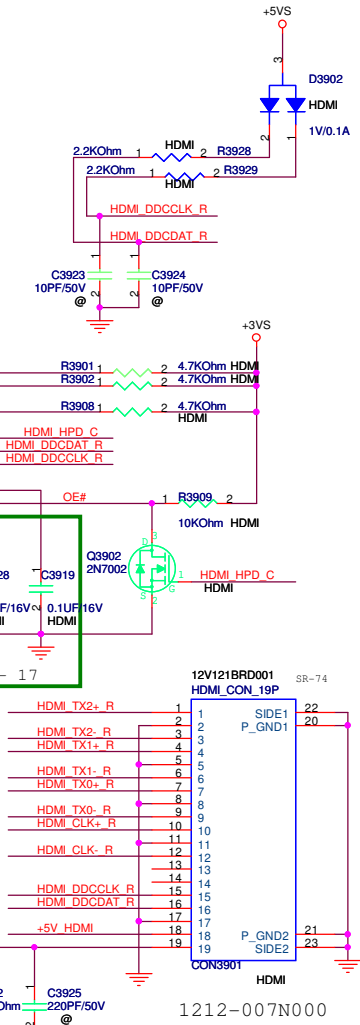
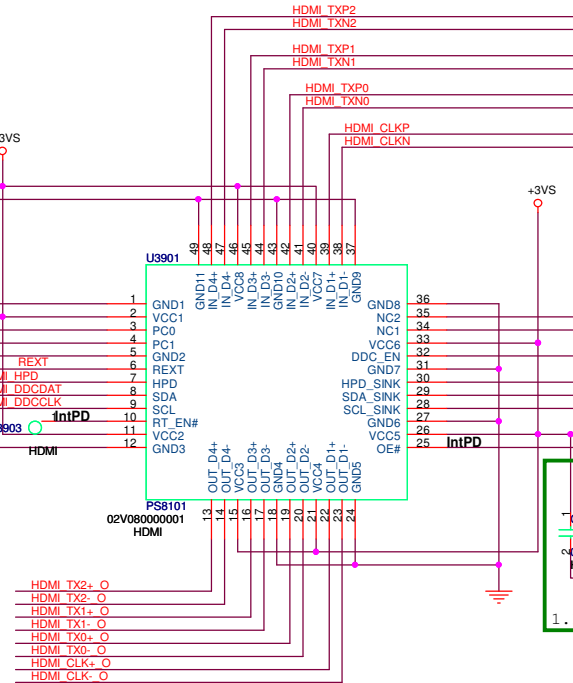
Vendor request



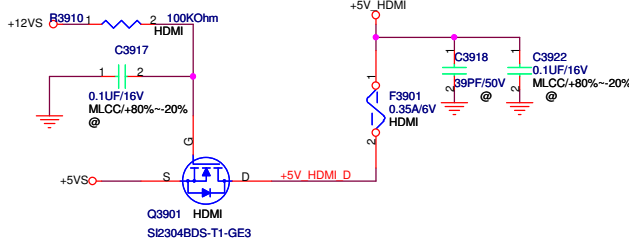
1.1 - 14



2.0 - 11



HDMI SPEC: 4.8~5.3V



<b>PEGATRON</b>		Title : <b>HDMI</b>	
BG1-HW RD Div.2-NB RD Dept.5		Engineer: <b>Johnson Huang</b>	
Size	Project Name	Rev	
Custom	<b>AIC70</b>	2.0	
Date: Wednesday, May 04, 2011	Sheet	39	of 77

WWW.AliSaler.Com

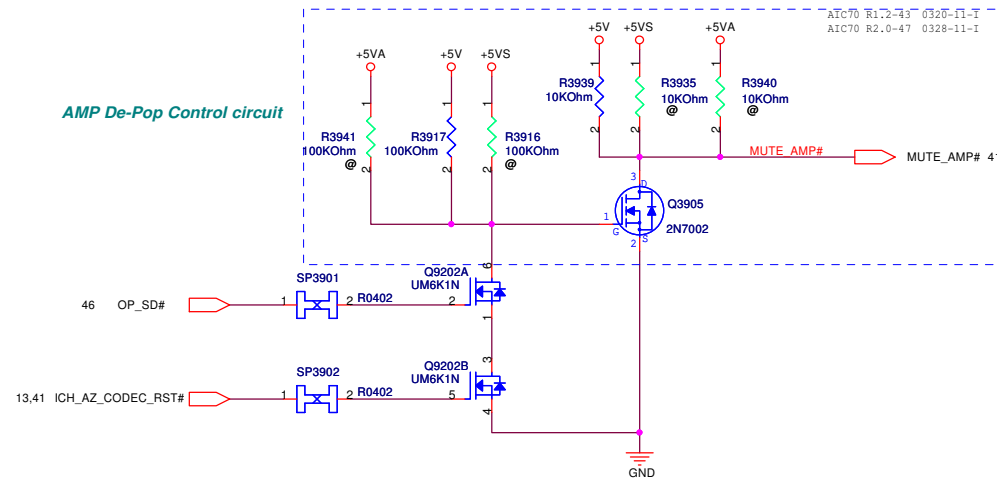




<b>PEGATRON</b>		Title : <i>Display Port</i>	
BU1-RD Div.1+HW RD Dept.1		Engineer: <i>Johnson Huang</i>	
Size Custom	Project Name <b>AIC70</b>		Rev 2.0
Date: <i>Wednesday, May 04, 2011</i>		Sheet	40 of 77

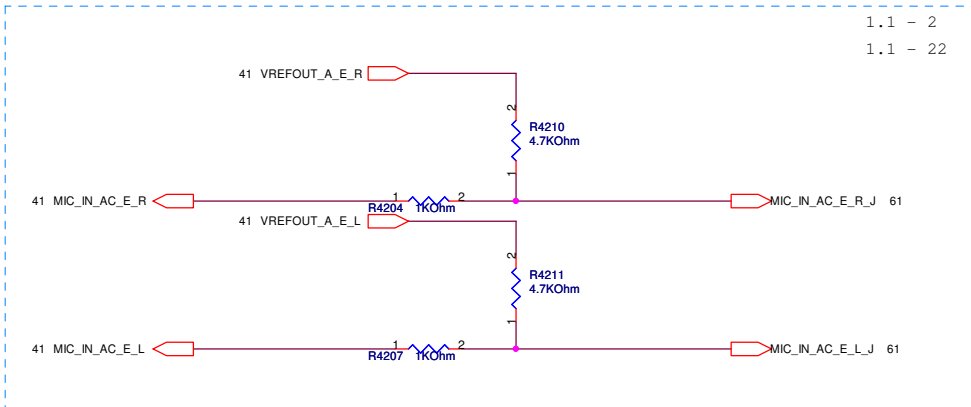


# AMP De-Pop Control circuit



# Modify De-Pop circuit

SR-43  
0125-11







Del Entry audio circuit

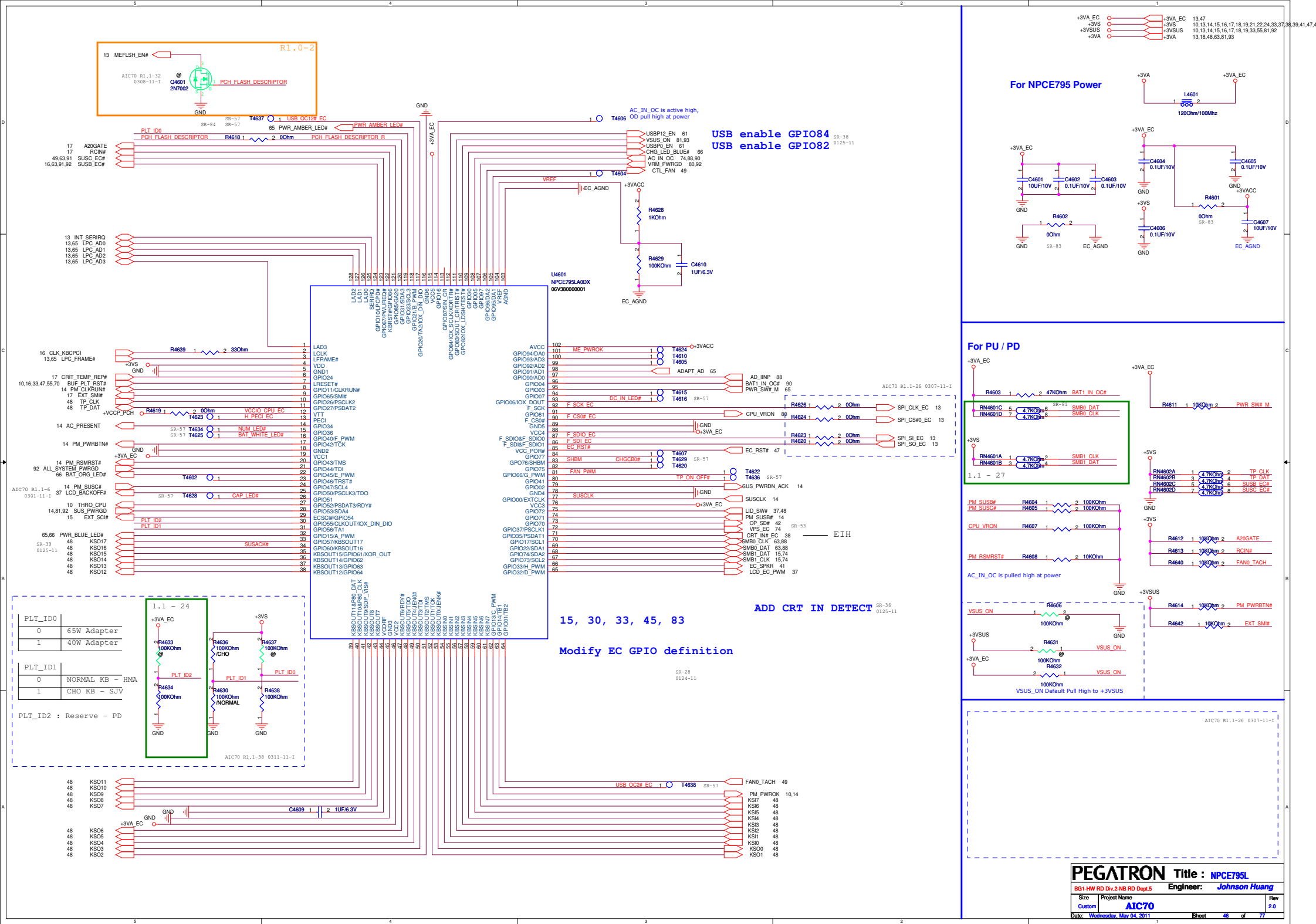
SR-8  
0121-11



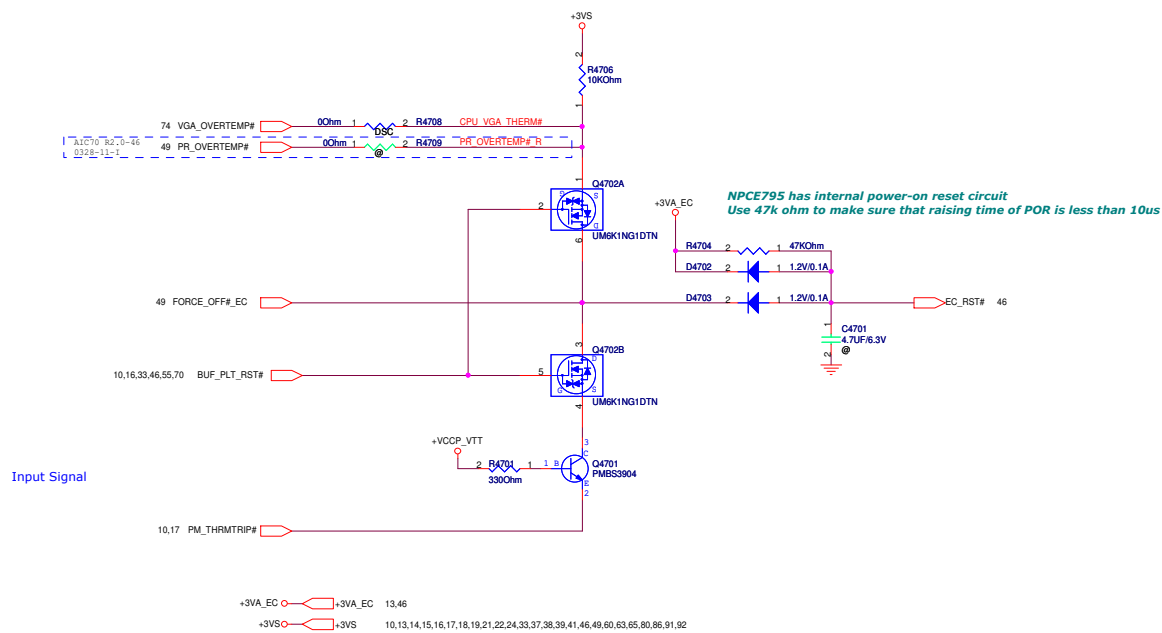
Del Entry audio circuit

SR-8  
0121-11

<b>PEGATRON</b>		Title : <b>AUDIO ALC269</b>	
BU1-RD Div.1-HW RD Dept.1		Engineer: <b>Johnson Huang</b>	
Size Custom	Project Name <b>AIC70</b>		Rev 2.0
Date: <b>Wednesday, May 04, 2011</b>		Sheet <b>45</b> of <b>77</b>	



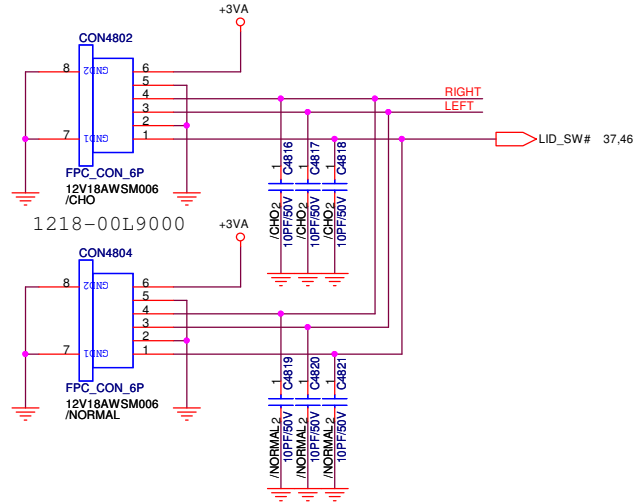
## Thermal Policy



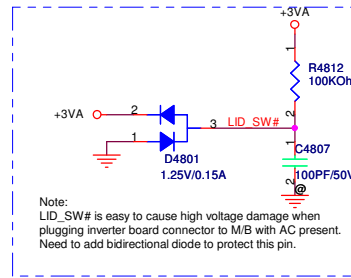


## Touch Pad Button/ Hall Sensor

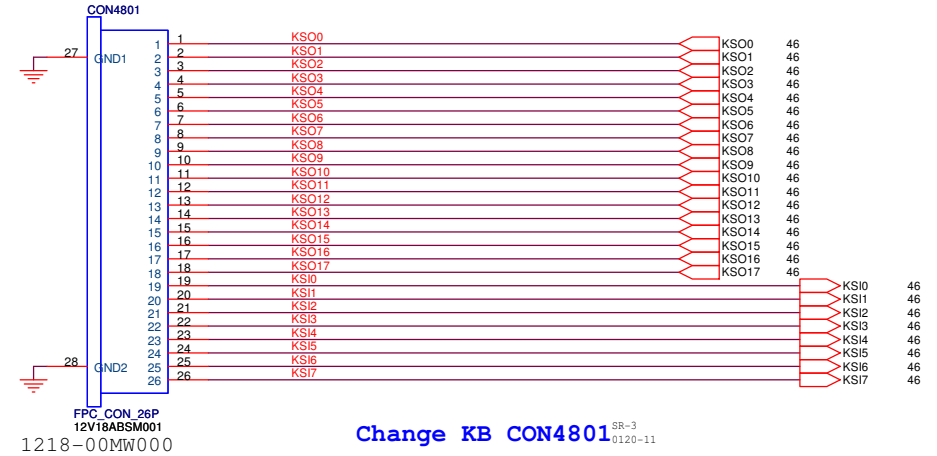
AIC70 R1.1-23 0306-11-I  
AIC70 R1.1-35 0309-11-I



close toU4601



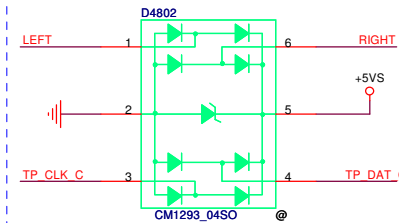
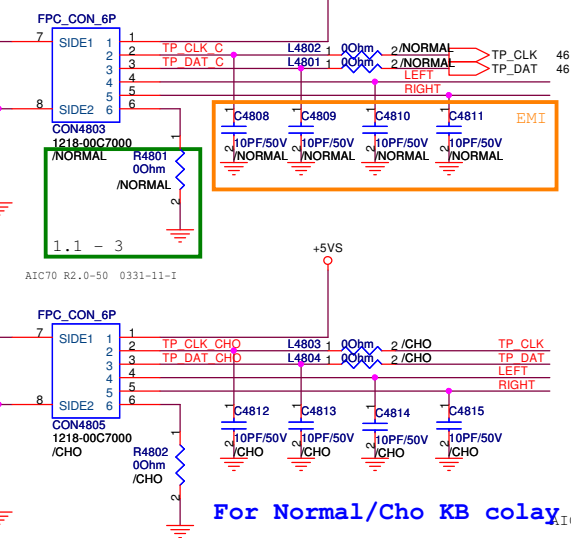
## Keyboard FOR 17"



Change KB CON4801 SR-3 0120-11

Change KB CON4801 PIN definition SR-25 0124-11  
Reverse KB CON4801 SR-19 SR-52 0124-11 0126-11

## Touch Pad



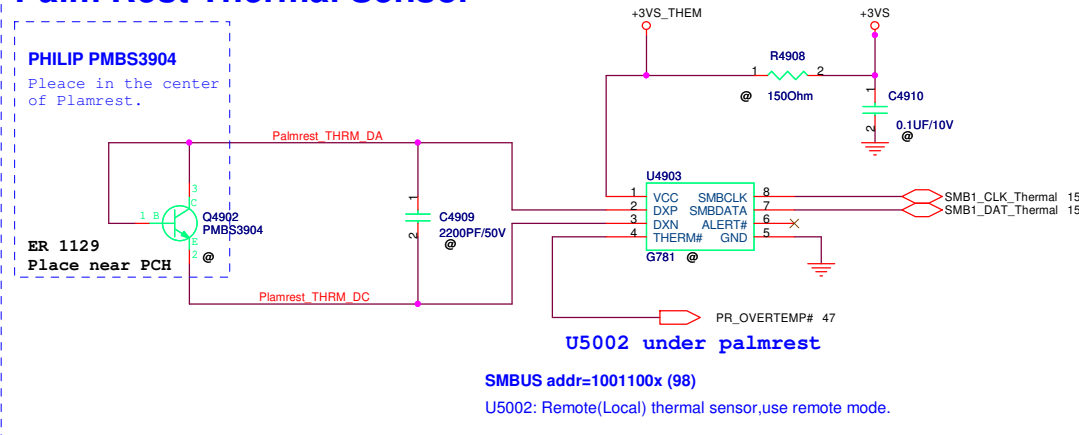
Remove 15'' KB connector AIC70 R1.1 - 1 0224-11 - I

Remove TP button circuit SR-22 0124-11

**PHILIP PMBS3904**  
Place in the center  
of Plamrest.

ER 1129  
Place near PCH

Q4902  
PMBS3904



(+3.2K: 85°C Protect +/- 3%)  
 (4.02K: 88°C Protect +/- 3%)  
 (3.6K: 92°C Protect +/- 3%)  
 (3K: 94~ 99°C Protect)

R4903  
 4.02KOhm  
 10Y220000069  
 1%

RT4901  
 10KOhm  
 3%

AIC70 R2.0-68  
 0504-11-1

+5V OP  
 C4904 2  
 0.1UF/16V

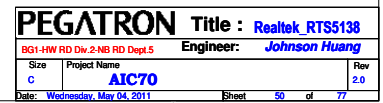
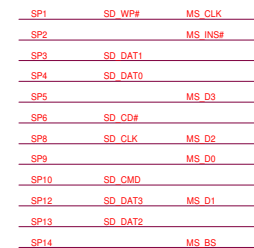
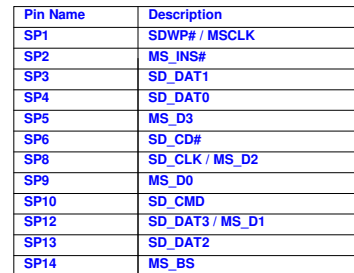
+5V A  
 R4906  
 100KOhm  
 @

Q4901  
 2N7002

U4902  
 NC2 VOUT  
 VDD  
 NC1 VSS  
 IC-PS78213NR  
 06V130000001

FORCE\_OFF#\_EC 47

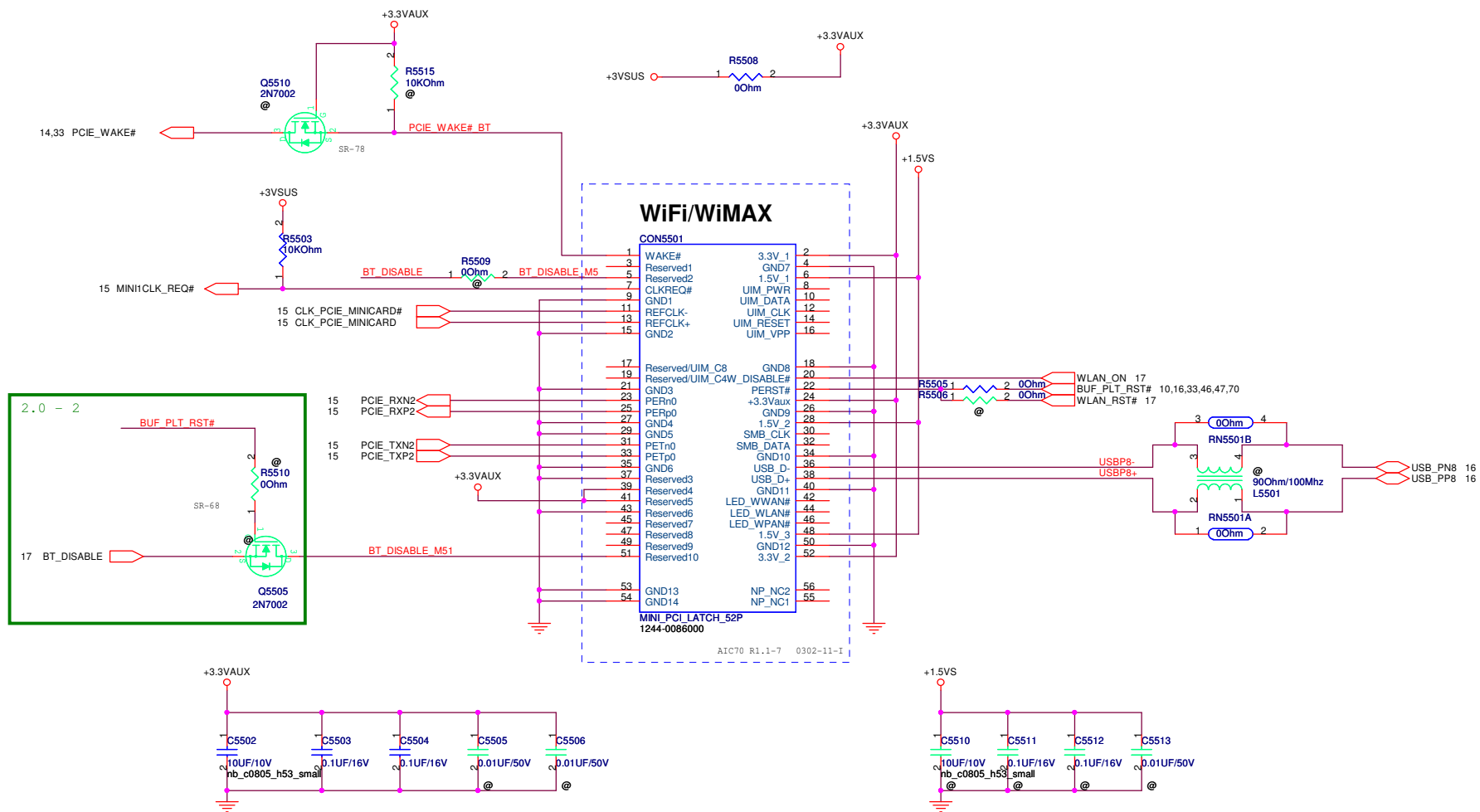
SUSC\_EC# 46,63,91







<b>PEGATRON</b>		Title : <b>PCIE NEW CARD</b>	
BU1-RD Div.1+HW RD Dept.1		Engineer: <b>Johnson Huang</b>	
Size Custom	Project Name <b>AIC70</b>		Rev 2.0
Date: <b>Wednesday, May 04, 2011</b>		Sheet	54 of 77





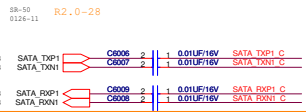
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BU1-RD Div.1-HW RD Dept.1		<b>Engineer:</b>	
Size	Project Name		Rev
Custom			2.0
Date:	Wednesday, May 04, 2011	Sheet	56 of 77



<b>PEGATRON</b>		Title : <b>MINICARD (WUSB /UPCONVERT)</b>	
BU1-RD Div.1-HW RD Dept.1		Engineer: <b>Johnson Huang</b>	
Size	Project Name		Rev
Custom	<b>AIC70</b>		2.0
Date: <b>Wednesday, May 04, 2011</b>		Sheet	57 of 77

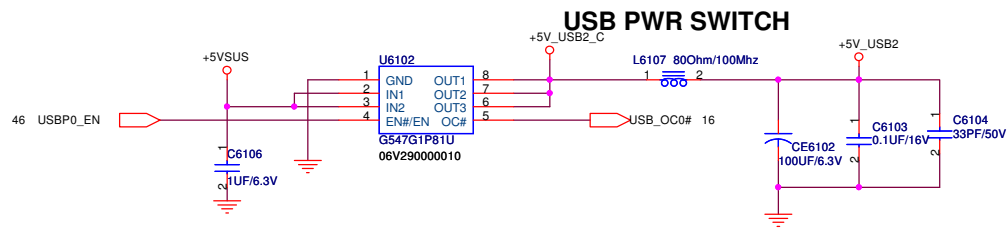


AIC70 R1.1-10 0304-11-I  
AIC70 R1.1-19 0306-11-I  
AIC70 R1.1-27 0307-11-I



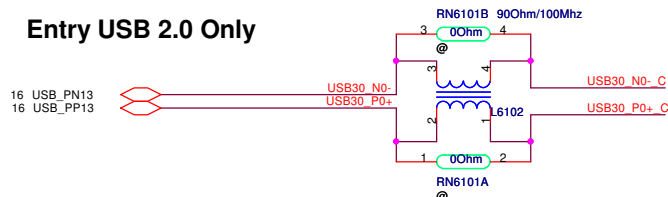
AIC70 R1.1 - 2  
0224-11 - I





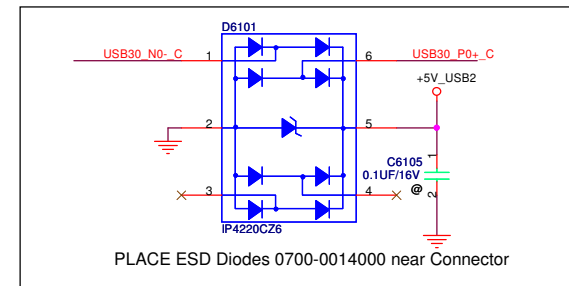
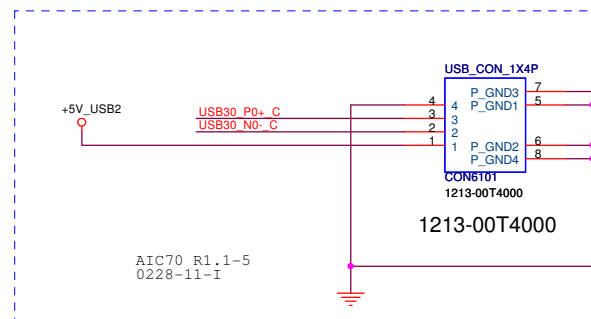
change USB power switch circuit SR~1 0120~11 SR~26 0124~11 SR~34 0125~11

### Entry USB 2.0 Only



Modify D6101, RN6101, RN6105, RN6106 SR~30 0125~11

## USB 2.0

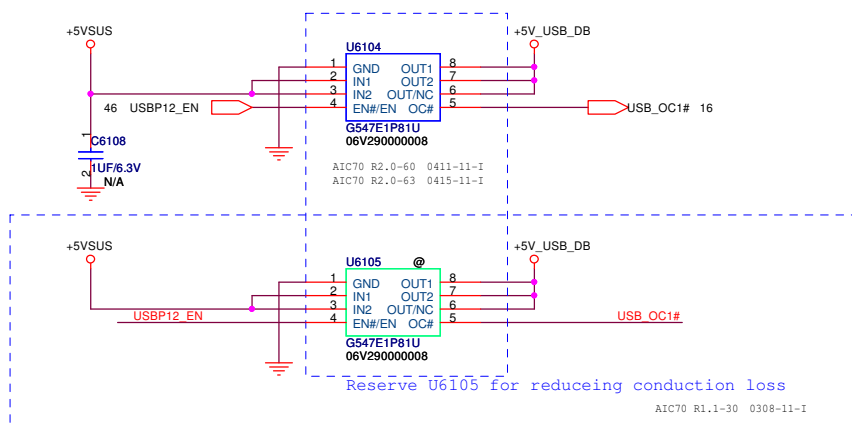


## USB Conn. for Entry colay HDMI USB 2.0

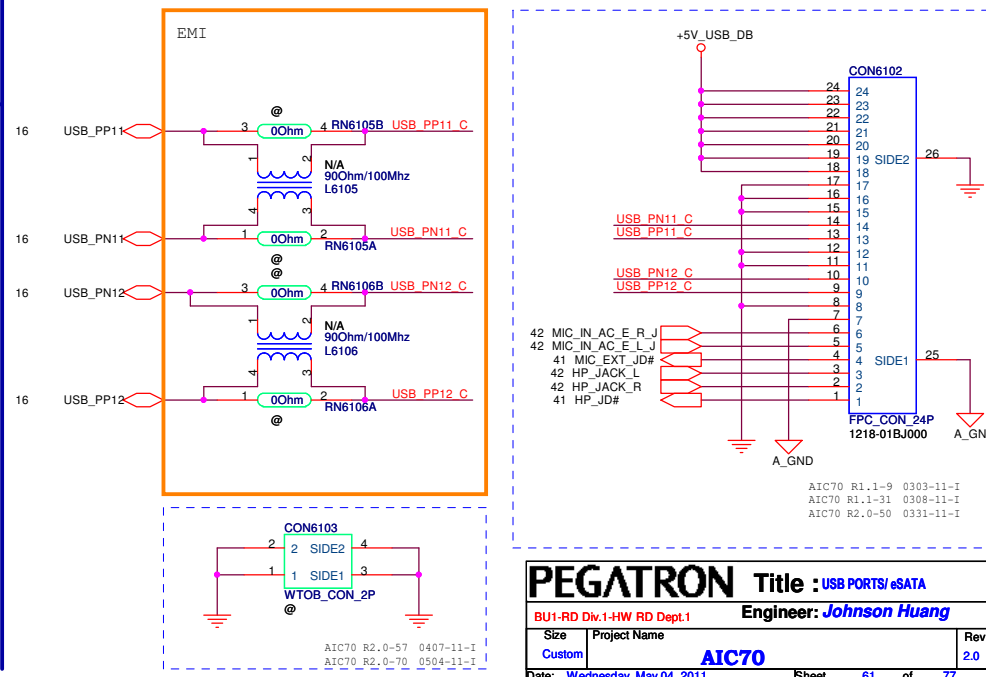
Remove USB\_9 (HDMI) SR~21 0124~11

### USB Power Switch for USB DB Main

change USB power switch circuit SR~26 0124~12 SR~38 0125~13



## AUDIO BOARD/w USB2.0 x2



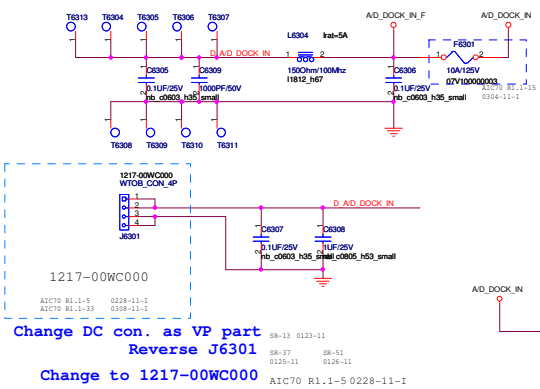
TouchPanel CON

Camera Module CON

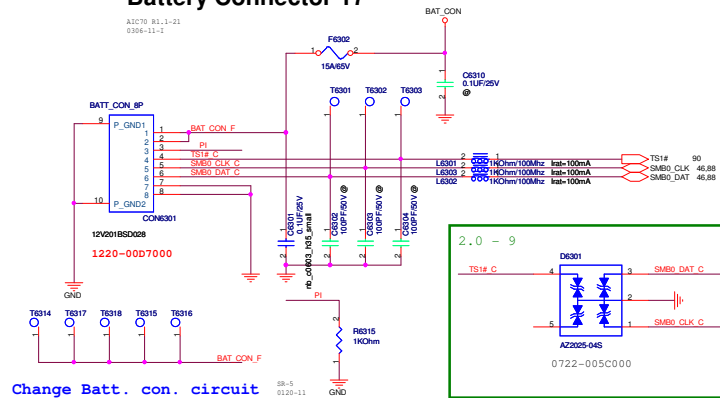
B/T MODULE

FELICA MODULE

**DC IN**

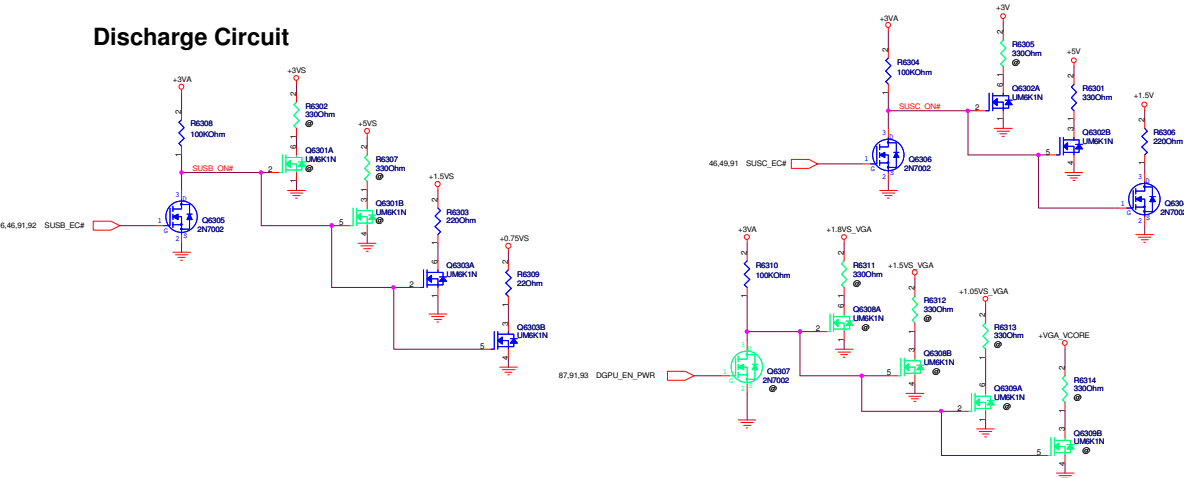


## Battery Connector 17"



**Remove 15'' Battery connector** AIC70 R1.1 - 1  
0224-11 - I

### Discharge Circuit



<b>PEGATRON</b>		Title : <u>DC-IN DISCHARGE</u>	
BU1-RD Div. 1-HW RD Dept.1		Engineer: <u>Johnson Huang</u>	
Size	Project Name	Rev	
Date	<b>AIC70</b>	2.0	
Custom: <u>Wednesday, May 04, 2011</u>		Sheet	63 of 77



Notes:  
BRAIDWOOD right angled Connector (1.8V keyed)  
Compatible BRAIDWOOD Modules  
1.8V Mobile NVM 4GB 31.60mm x21.5mm  
1.8V Mobile NVM 8GB 31.60mm x 21.5mm  
1.8V Mobile NVM 16GB 31.60mm x 32.5mm

<b>PEGATRON</b>		Title : <i>NVM</i>	
BU1-RD Div.1+HW RD Dept.1		Engineer: <i>Johnson Huang</i>	
Size Custom	Project Name <b>AIC70</b>		Rev 2.0
Date: <i>Wednesday, May 04, 2011</i>		Sheet <i>64</i> of <i>77</i>	



# LED (Main)

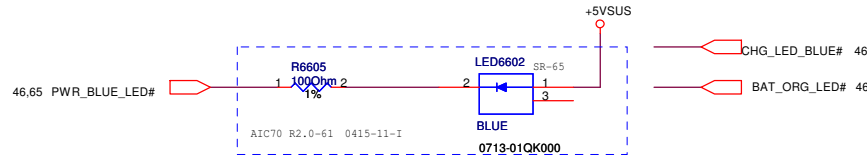
Left

Right

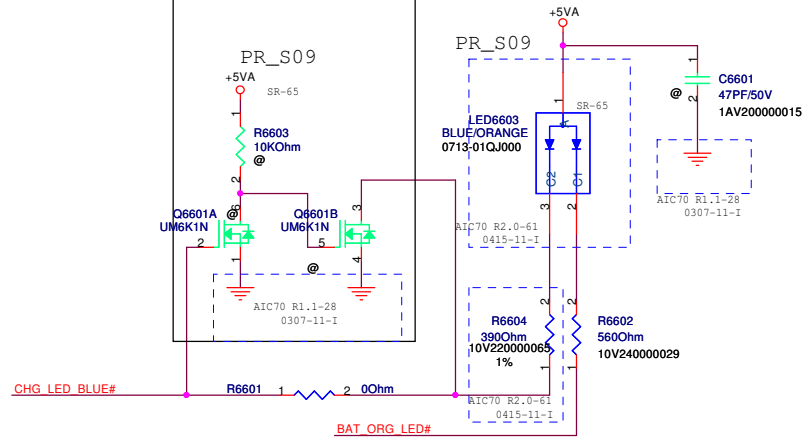


Battery

Power LED



Charger LED



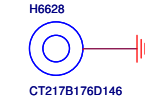
Remover LED circuit

Modify LED circuit

SR-18  
0124-11  
SR-39  
0125-11

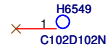
WLAN NUT

PCH Local Side Symbol

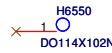


SR-69

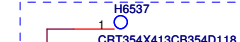
Fix hole



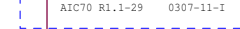
Detail C



Screw Ax10



AIC70 R1.1-29 0307-11-I



AIC70 R1.1-29 0307-11-I



AIC70 R1.1-29 0307-11-I



AIC70 R1.1-29 0307-11-I



AIC70 R1.1-29 0307-11-I



AIC70 R1.1-29 0307-11-I



AIC70 R1.1-29 0307-11-I



AIC70 R1.1-29 0307-11-I



AIC70 R1.1-29 0307-11-I



AIC70 R1.1-29 0307-11-I



AIC70 R1.1-29 0307-11-I



AIC70 R1.1-29 0307-11-I



AIC70 R1.1-29 0307-11-I



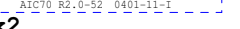
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AIC70 R1.1-29 0307-11-I



AIC70 R1.1-29 0307-11-I



AIC70 R1.1-29 0307-11-I



AIC70 R1.1-29 0307-11-I



AIC70 R1.1-29 0307-11-I



AIC70 R1.1-29 0307-11-I



AIC70 R1.1-29 0307-11-I



AIC70 R1.1-29 0307-11-I



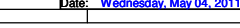
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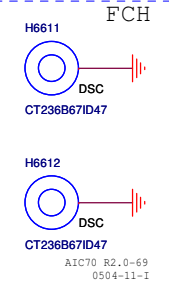
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AIC70 R1.1-29 0307-11-I



AIC70 R1.1-29 0307-11-I



AIC70 R2.0-69 0504-11-I



AIC70 R2.0-69 0504-11-I



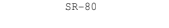
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AIC70 R2.0-69 0504-11-I



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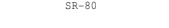
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AIC70 R2.0-69 0504-11-I



AIC70 R2.0-69 0504-11-I



AIC70 R2.0-69 0504-11-I



AIC70 R2.0-69 0504-11-I



AIC70 R2.0-69 0504-11-I



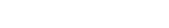
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AIC70 R2.0-69 0504-11-I



AIC70 R2.0-69 0504-11-I



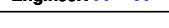
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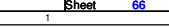
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AIC70 R2.0-69 0504-11-I

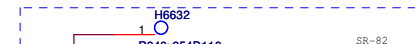


AIC70 R2.0-69 0504-11-I



AIC70 R2.0-69 0504-11-I

Screw Fx2



AIC70 R1.1-29 0307-11-I



AIC70 R1.1-29 0307-11-I



AIC70 R1.1-29 0307-11-I



AIC70 R1.1-29 0307-11-I



AIC70 R1.1-29 0307-11-I



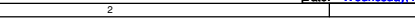
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AIC70 R1.1-29 0307-11-I



AIC70 R1.1-29 0307-11-I



AIC70 R1.1-29 0307-11-I

PEGATRON Title : LED CIR/FW SCREW

BU1-RD Div.1-HW RD Dept.1 Engineer: Johnson Huang

Size Project Name

Custom AIC70

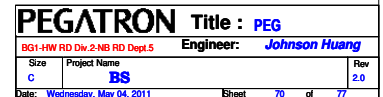
Date: Wednesday, May 04, 2011

Sheet 66 of 77

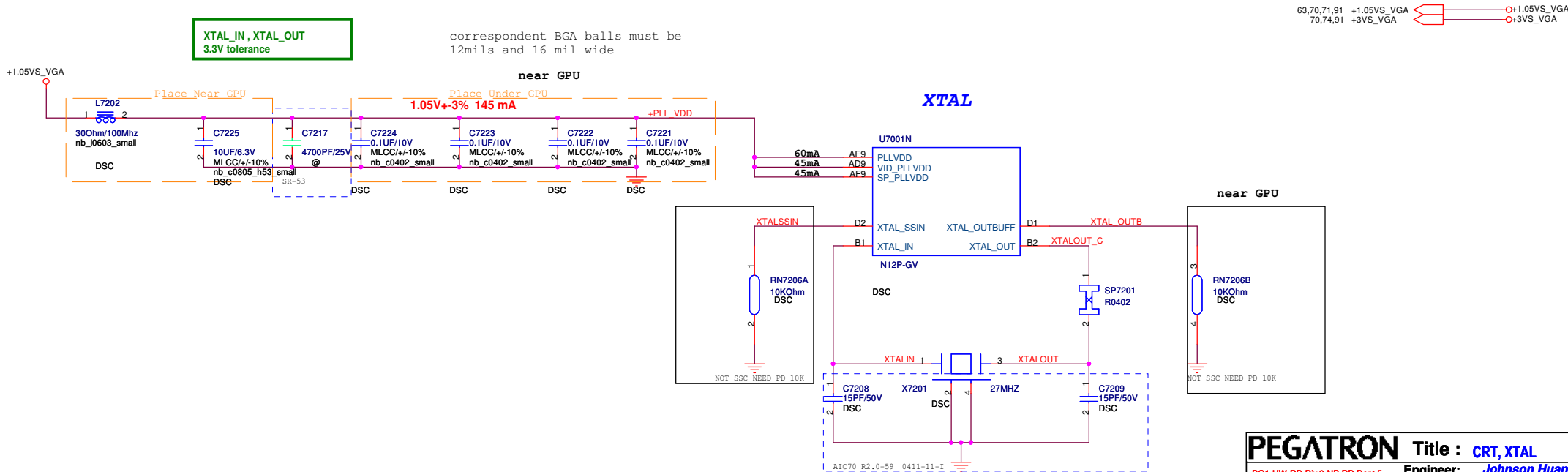
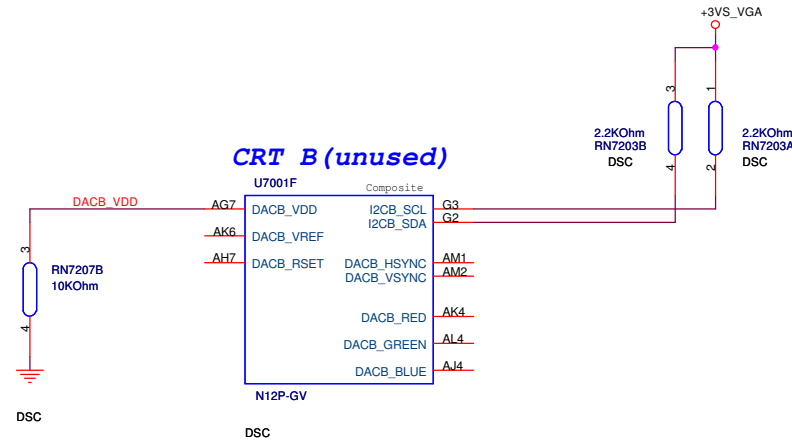
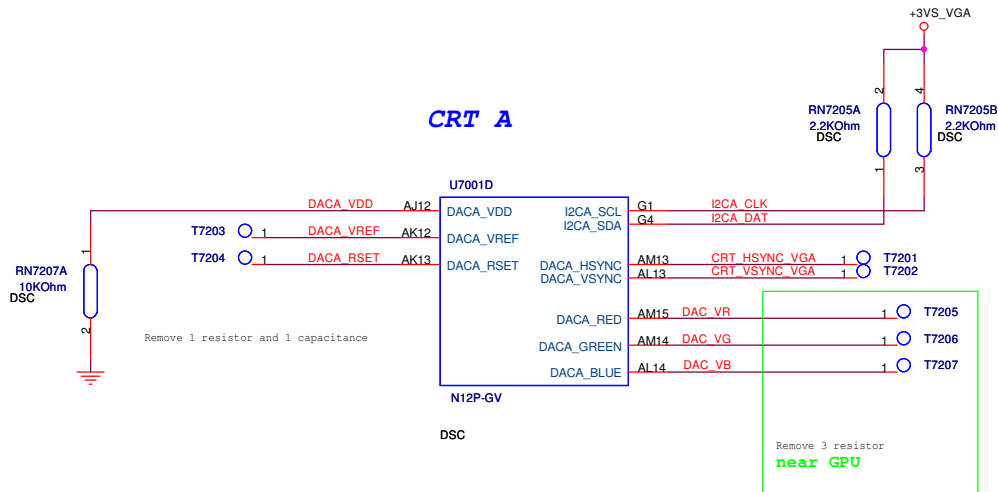


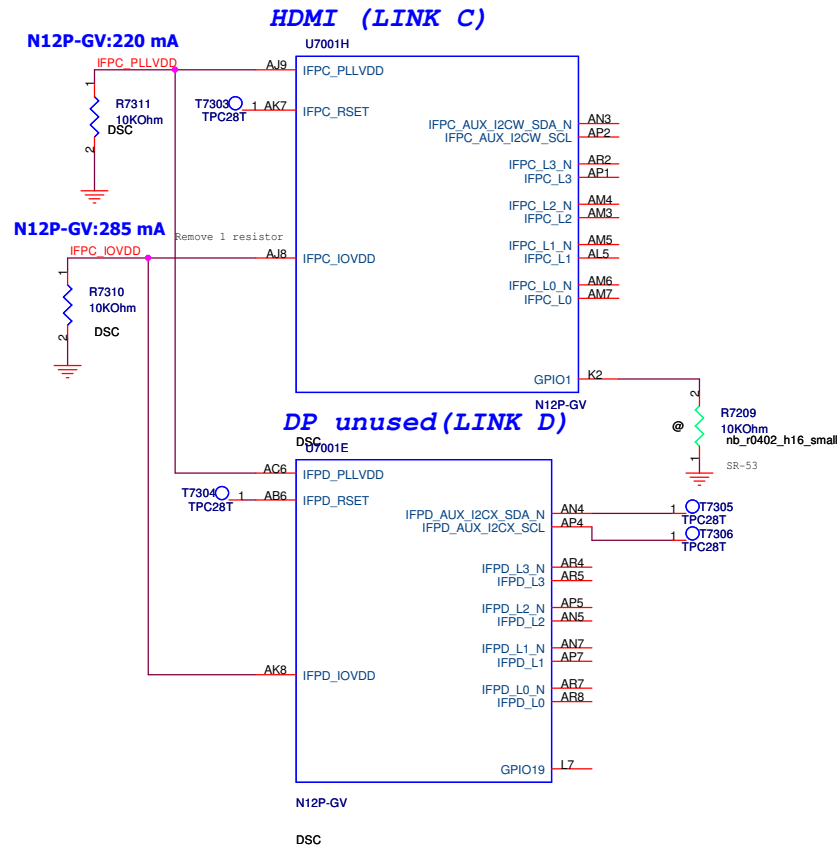
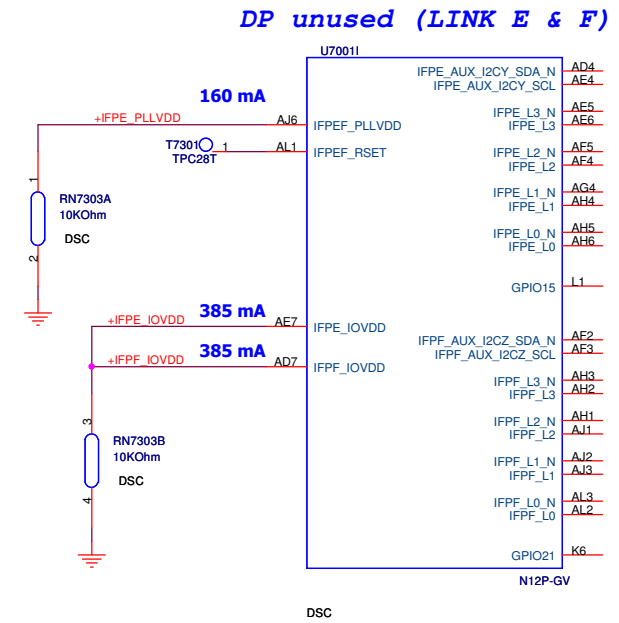
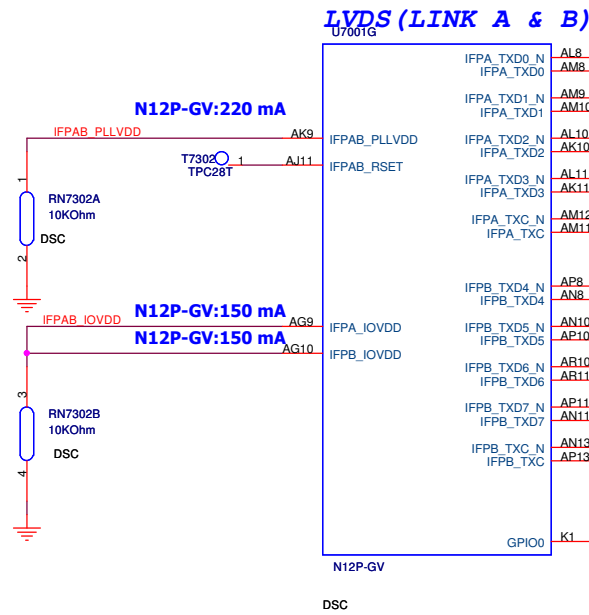
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BU1-RD Div.1+HW RD Dept.1		Engineer: Johnson Huang	
Size	Project Name		Rev
Custom			2.0
Date: Wednesday, May 04, 2011		Sheet	69 of 77







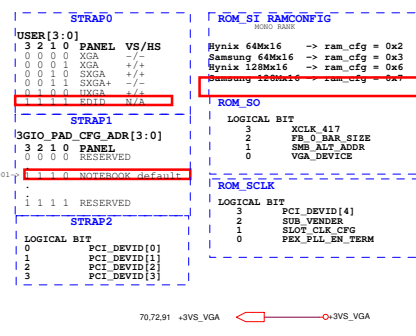
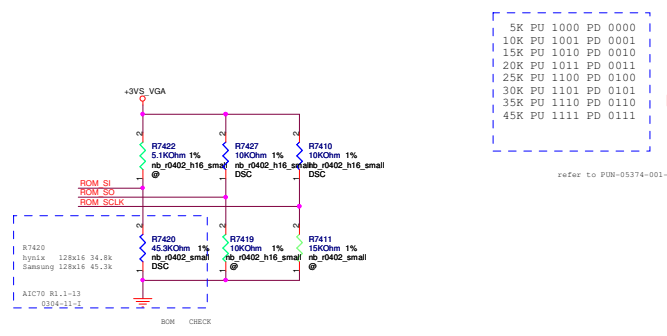
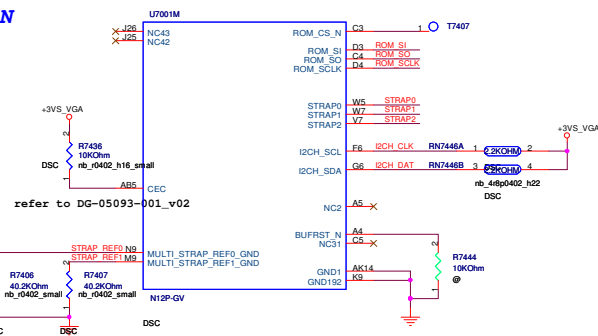




IFPx	A	B	C	D	E	F
TURKEY	LVDS A	LVDS B	HDMI	unused		

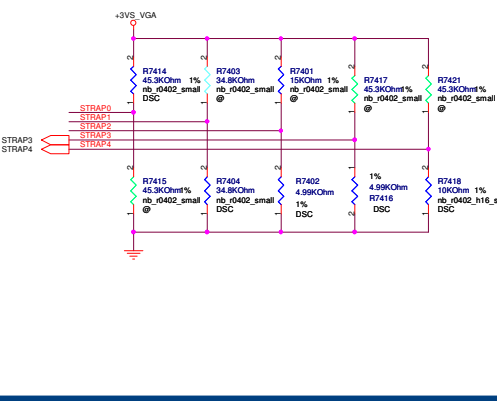
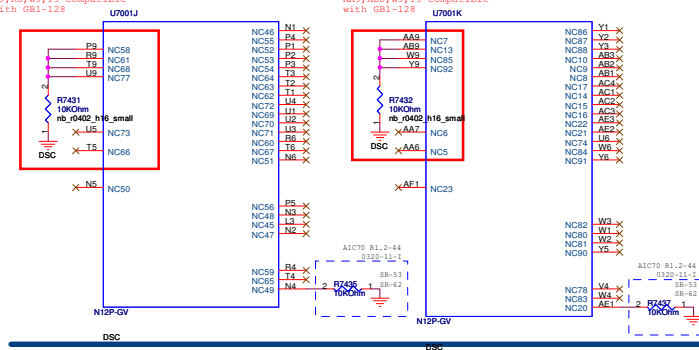
63,70,71,72,91 +1.05VS\_VGA  
63,91 +1.8VS\_VGA  
70,72,74,91 +3VS\_VGA

## STRAP PIN



Muti I/O unused

9,R8,W9,T9 Compatible  
with GB1-128



			N12P-LP QS		N12P-GV ES		N12M-GE QS	
			PU	PD	PU	PD	PU	PD
ROM_SO	R7427	R7419	@	10K	@	10K	@	10K
ROM_SCLK	R7410	R7411	@	15K	@	15K	@	15K
ROM_SI	R7422	R7420	@	H 64:15K S 64:20K	@	H 64:15K S 64:20K	@	H 64:15 S 64:20
Strap2	R7401	R7402	25K	@	45K	@	15K	@
Strap1	R7403	R7404	@	35K	@	35K	@	35K
Strap0	R7414	R7415	45K	@	45K	@	45K	@
Strap3	R7417	R7416	@	@	@	20k	@	@
Strap4	R7421	R7418	@	@	@	10k	@	@

GPIO, THERM, SMBUS, JTAG, LVDS MISC, GPU\_VID

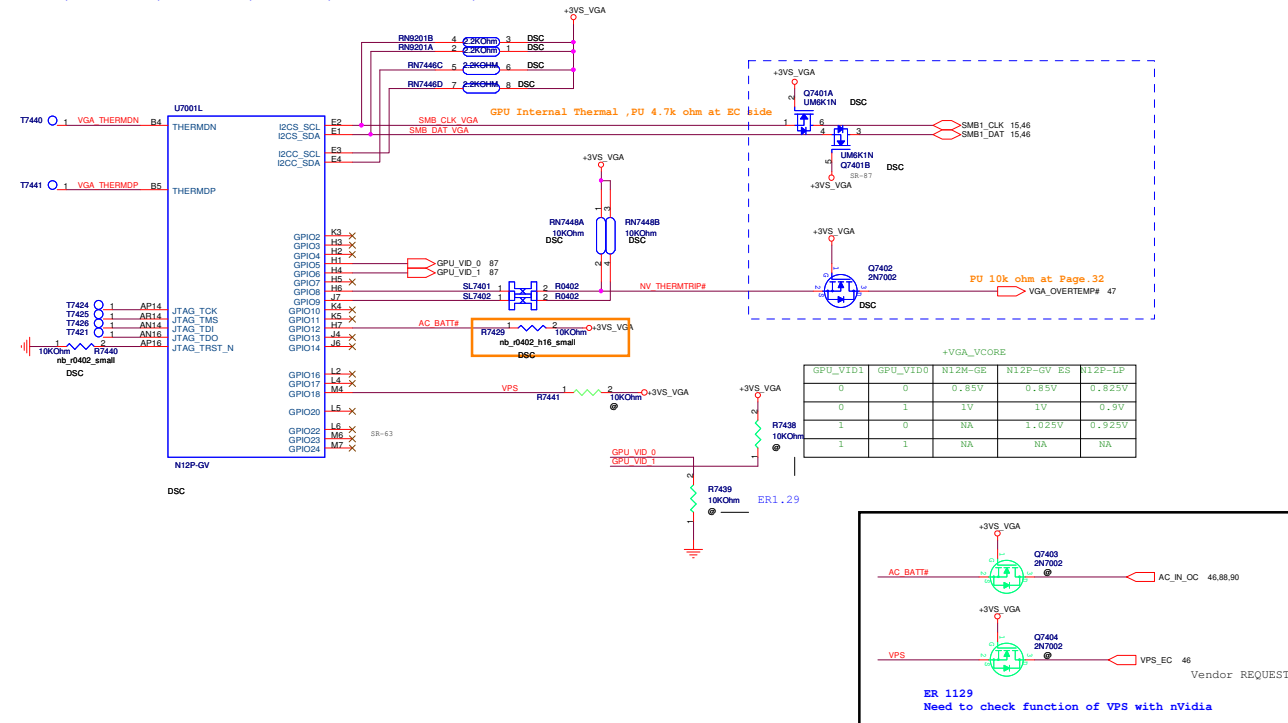
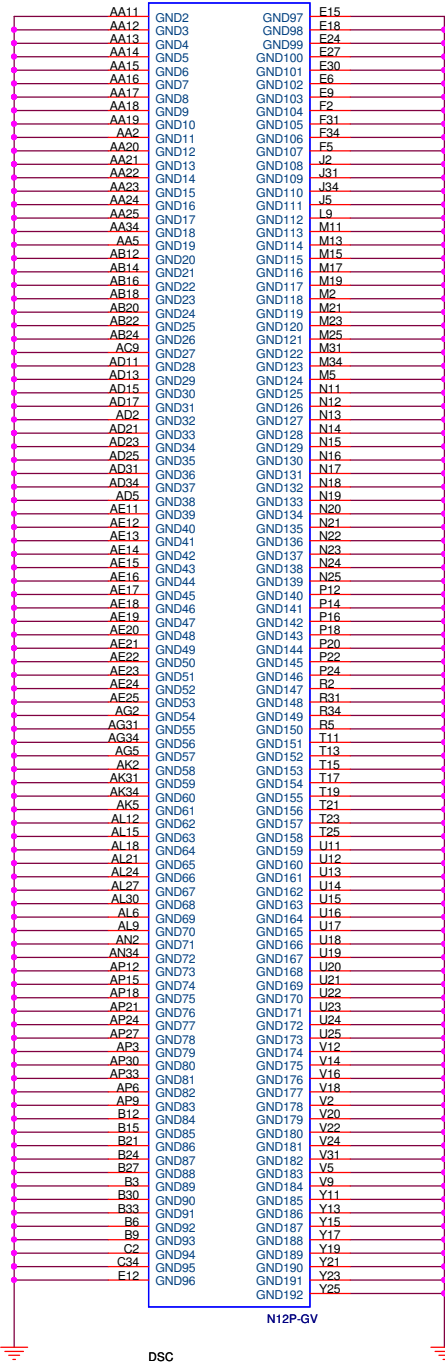


Table 12.1 GPIO Description

GPIO PIN Name	Normal Function	I/O	Functional Description
GPIO0	General Purpose		
GPIO1	HPD_C	I	Hot Plug Detect for IPFC
GPIO2	LCDD_BL_PWM	O	Panel Backlight Brightness Control (PWM capable)
GPIO3	LCDD_VCC	O	Panel Power Enable
GPIO4	LCDD_BLEN	O	Panel Backlight ON/OFF Control (PWM capable)
GPIO5	GPU_VID0	O	GPU Core VDD VID0
GPIO6	GPU_VID1	O	GPU Core VDD VID1
GPIO7	GPU_VID2	O	GPU Core VDD VID2
GPIO8	OVERT	I/O	Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Thermal Alert
GPIO10	MEM_VREF_CTL	O	Memory VREF Control
GPIO11	SLI_RASTER_SYNC	I/O	SLI Raster Sync
GPIO12	PWR_LEVEL	I	AC Power Detect Input
GPIO13	THERM_LOAD_STEP_DOWN	O	Power Supply Control
GPIO14	THERM_LOAD_STEP_UP	O	Power Supply Control
GPIO15	HPD_E	I	Hot Plug Detect for IPFE
GPIO16	FAN_PWM	O	Programmable Fan Control
GPIO17	Reserved		
GPIO18	Reserved		
GPIO19	HPD_D	I	Hot Plug Detect for IPFD
GPIO20	Reserved		
GPIO21	HPD_F	I	Hot Plug Detect for IPFF
GPIO22	SWAPRDY	I	SLI Swap Ready Signal
GPIO23	3Dvision	O	3Dvision functions
GPIO24	General Purpose		

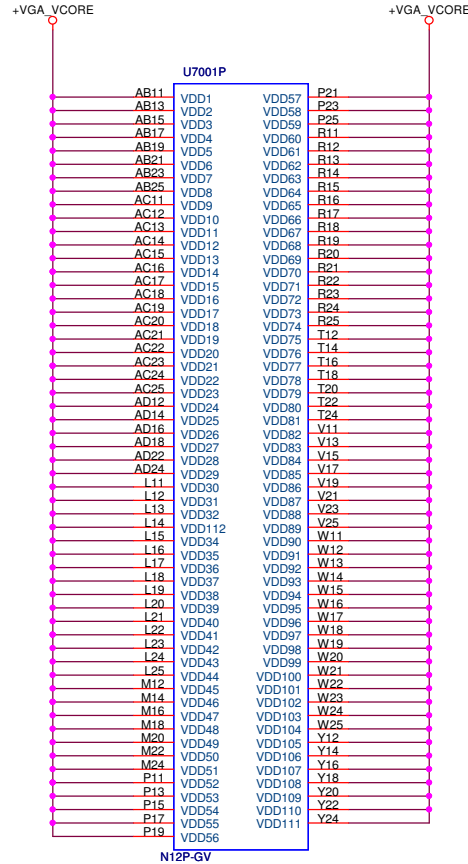
GND

U7001O

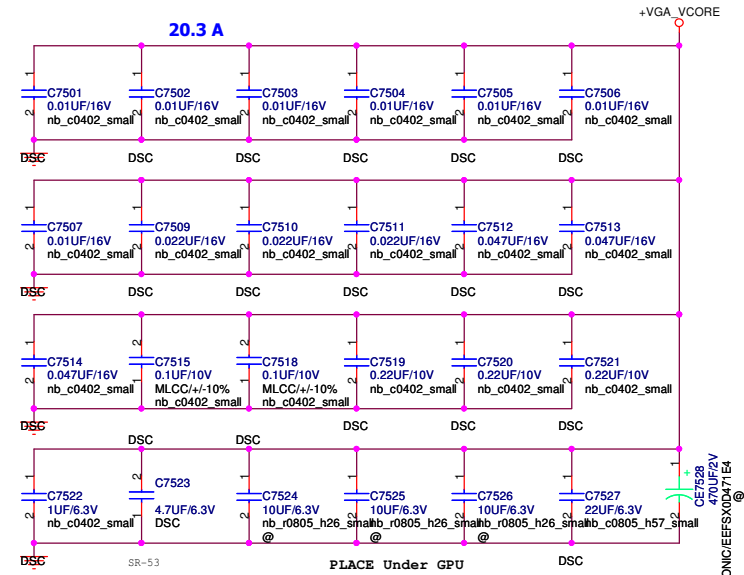


VAG\_VCORE

U7001P



20.3 A



PANASONIC/EEFSX0471EA

63.87 +VGA\_VCORE

**\*TOP SIDE\***

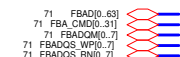


Table 5.4 Mode E Command Mapping

M12x Fermi DDR3 mode E	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	ODT	
FBx_CMD1	CS1*	
FBx_CMD2	CS0*	
FBx_CMD3	CKE	
FBx_CMD4	A9	A11
FBx_CMD5	A6	A7
FBx_CMD6	A3	BA1
FBx_CMD7	A0	A12
FBx_CMD8	A8	AB
FBx_CMD9	A12	A0
FBx_CMD10	A1	A2
FBx_CMD11	RAS*	RAS*
FBx_CMD12	A13	A14
FBx_CMD13	BA1	A3
FBx_CMD14	A4	A13
FBx_CMD15	CSA*	CSA*
FBx_CMD16		CKE
FBx_CMD17		CS1*
FBx_CMD18		CS0*
FBx_CMD19		ODT
FBx_CMD20	RST	RST
FBx_CMD21	A7	A6
FBx_CMD22	A4	A5
FBx_CMD23	A11	A9
FBx_CMD24	A2	A1
FBx_CMD25	A10	WE*
FBx_CMD26	A5	A4
FBx_CMD27	BA2	A15
FBx_CMD28	WE*	A10
FBx_CMD29	BA0	BA0
FBx_CMD30	A15	BA2
FBx_CMD31		

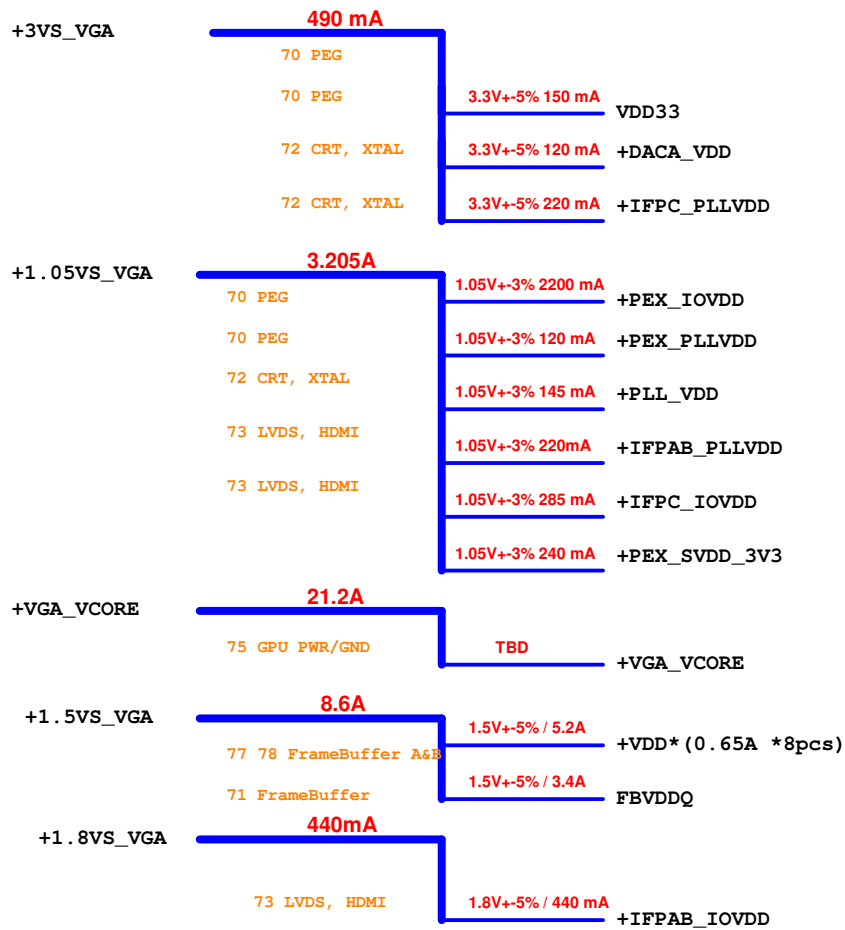
**\*TOP SIDE\***



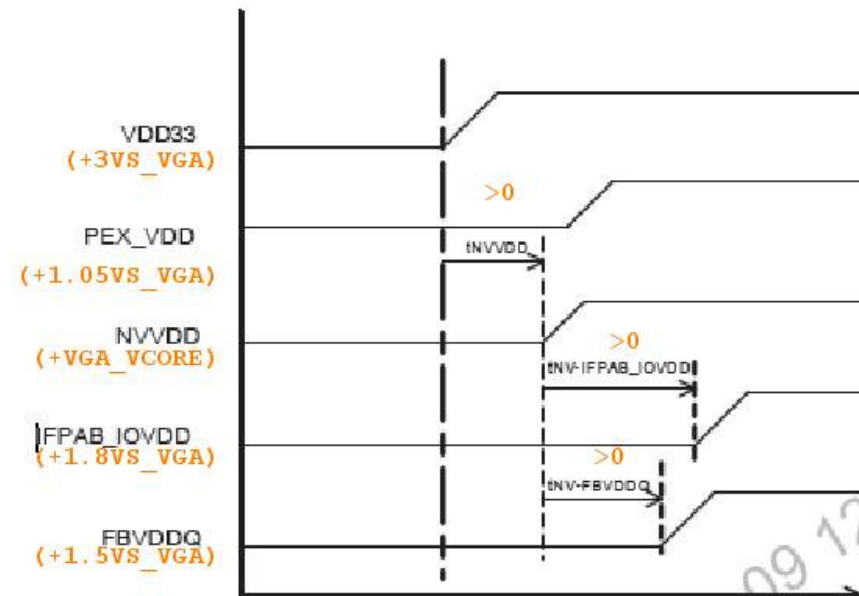
Del B channel VRAM \* 4 circuit

SR-10  
0121-11





**N12P-LP Total:40W (w/VRAM)**



**Figure 3.20 Recommended Power On Sequencing Order**

**Power Up Sequence :**  
 +3VS\_VGA -> +1.05VS\_VGA -> +VGA\_VCORE -> +1.5VS\_VGA -> +1.8VS\_VGA

**Power Down Sequence :**  
 +1.8VS\_VGA -> +1.5VS\_VGA -> +VGA\_VCORE -> 1.05VS\_VGA -> +3VS\_VGA

according to Page 63, DG-05093-001\_v02



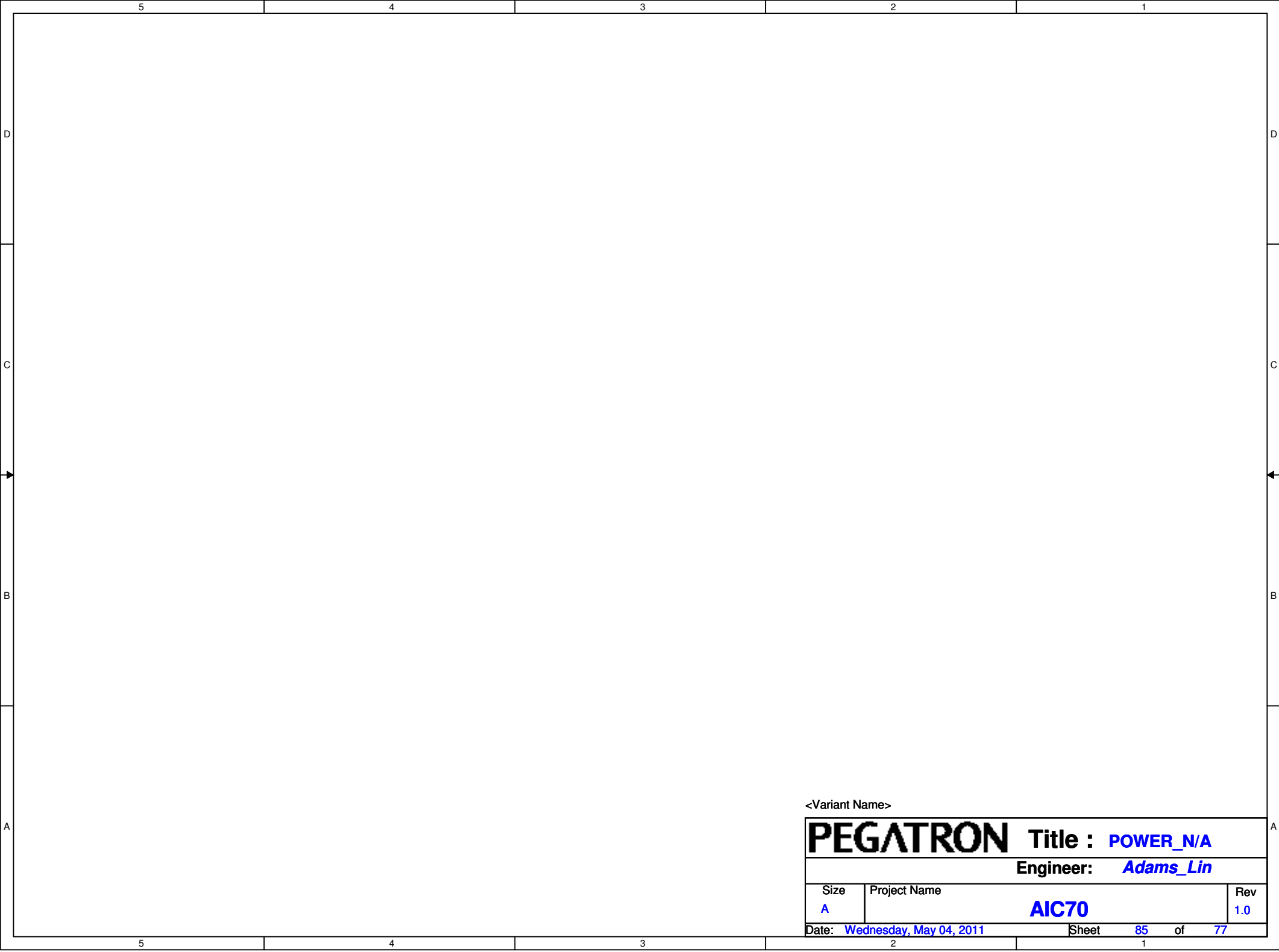






<Variant Name>

<b>PEGATRON</b>		<b>Title :</b>	<b>POWER_N/A</b>
		<b>Engineer:</b>	<b>Adams_Lin</b>
Size <b>Custom</b>	Project Name <b>AIC70</b>	Rev <b>1.0</b>	
Date: <b>Wednesday, May 04, 2011</b>	Sheet <b>1</b>	<b>84</b>	of <b>77</b>



<Variant Name>

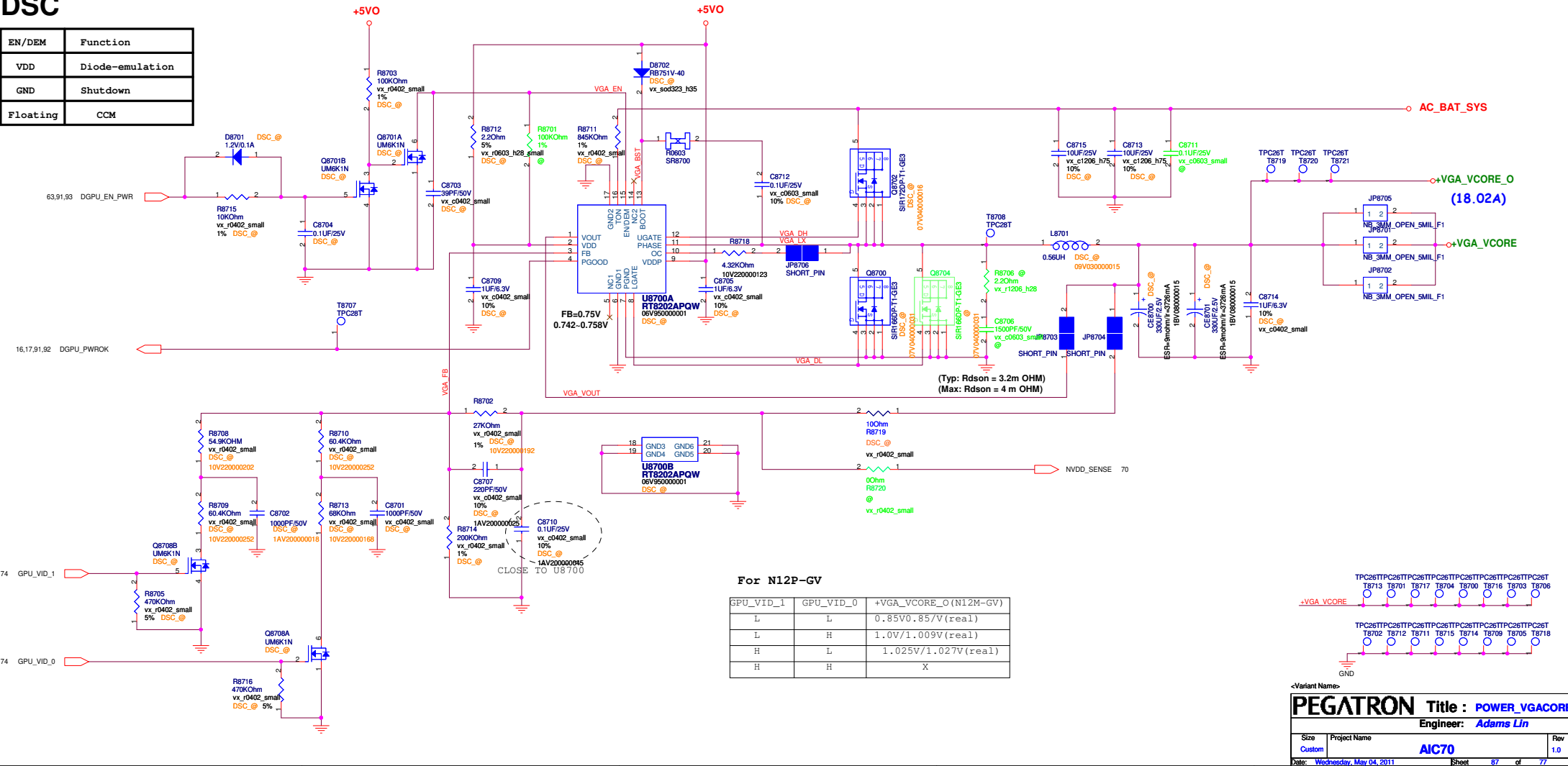
<b>PEGATRON</b>		Title : <b>POWER_N/A</b>	
Engineer: <b>Adams_Lin</b>			
Size <b>A</b>	Project Name <b>AIC70</b>		Rev <b>1.0</b>
Date: <b>Wednesday, May 04, 2011</b>		Sheet	<b>85</b> of <b>77</b>



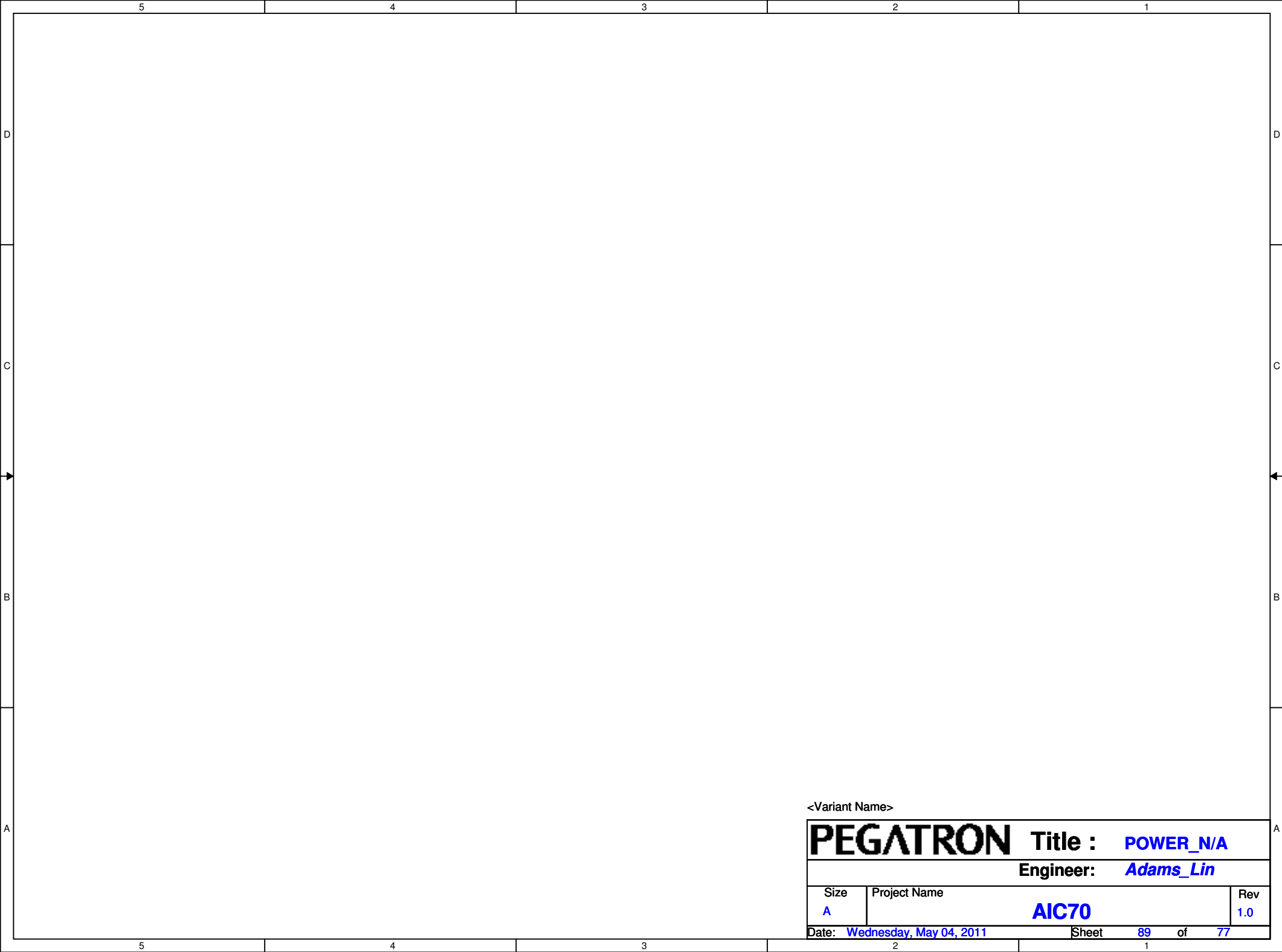


DSC

EN/DEM	Function
VDD	Diode-emulation
GND	Shutdown
Floating	CCM



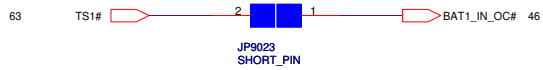




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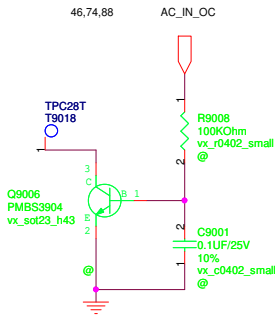
<b>PEGATRON</b>		Title : <b>POWER_N/A</b>	
		Engineer: <b>Adams_Lin</b>	
Size <b>A</b>	Project Name <b>AIC70</b>		Rev <b>1.0</b>
Date: <b>Wednesday, May 04, 2011</b>		Sheet	<b>89</b> of <b>77</b>

BATTERY IN DETECT

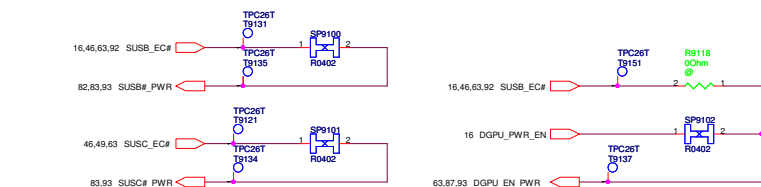
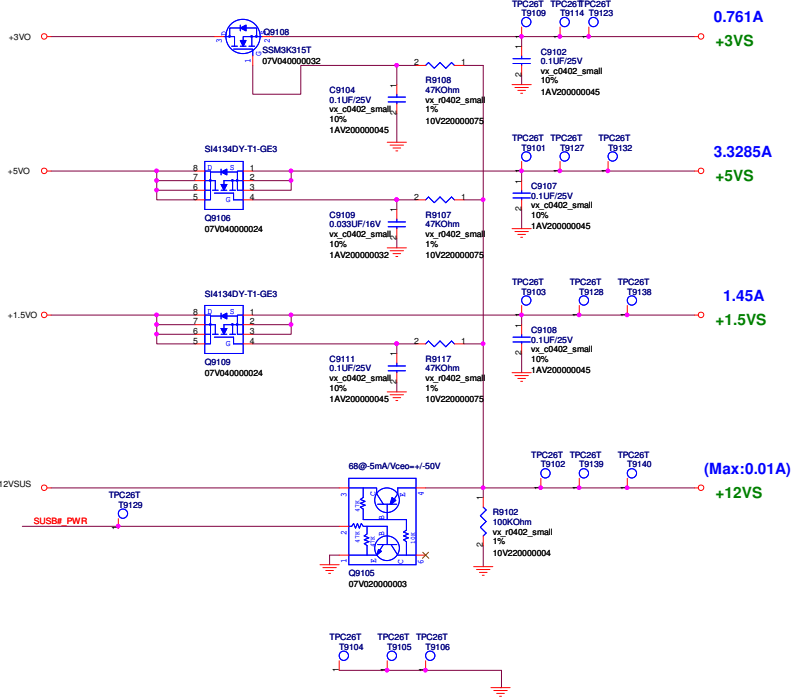


ADAPTER IN DETECT

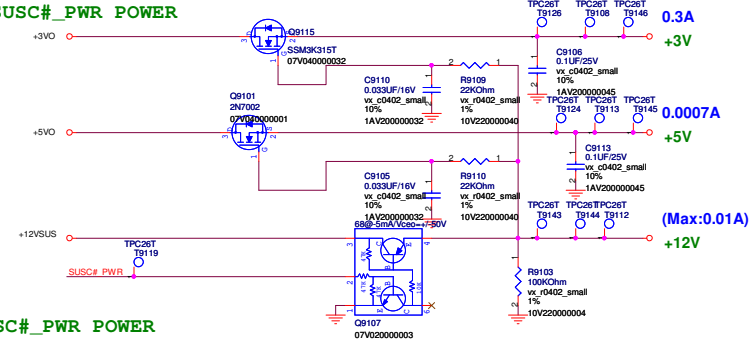
Use MAX17015 IC function to Cost down component



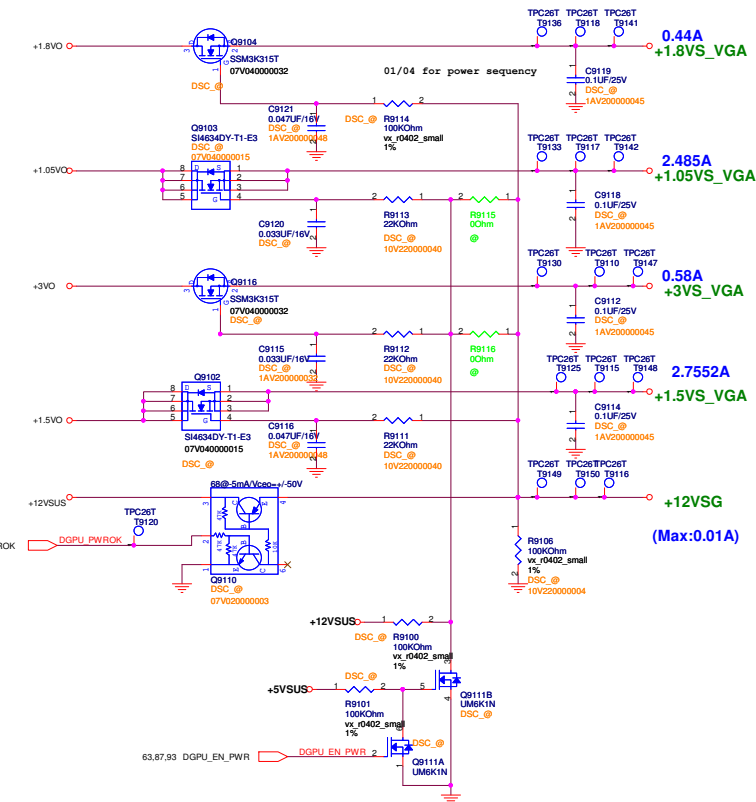
## SUSB#\_PWR POWER



## SUSC#\_PWR POWER



## DSC#\_PWR POWER



Ron = 41.5 mΩ (max) (BVGS = 4.5 V)  
Ron = 27.6 mΩ (max) (BVGS = 10 V)

NOTE: +3V=0.3A(EE)+1.4978A(+3V Provide to 1.8V PWR)=1.7978A

&lt;Variant Name&gt;

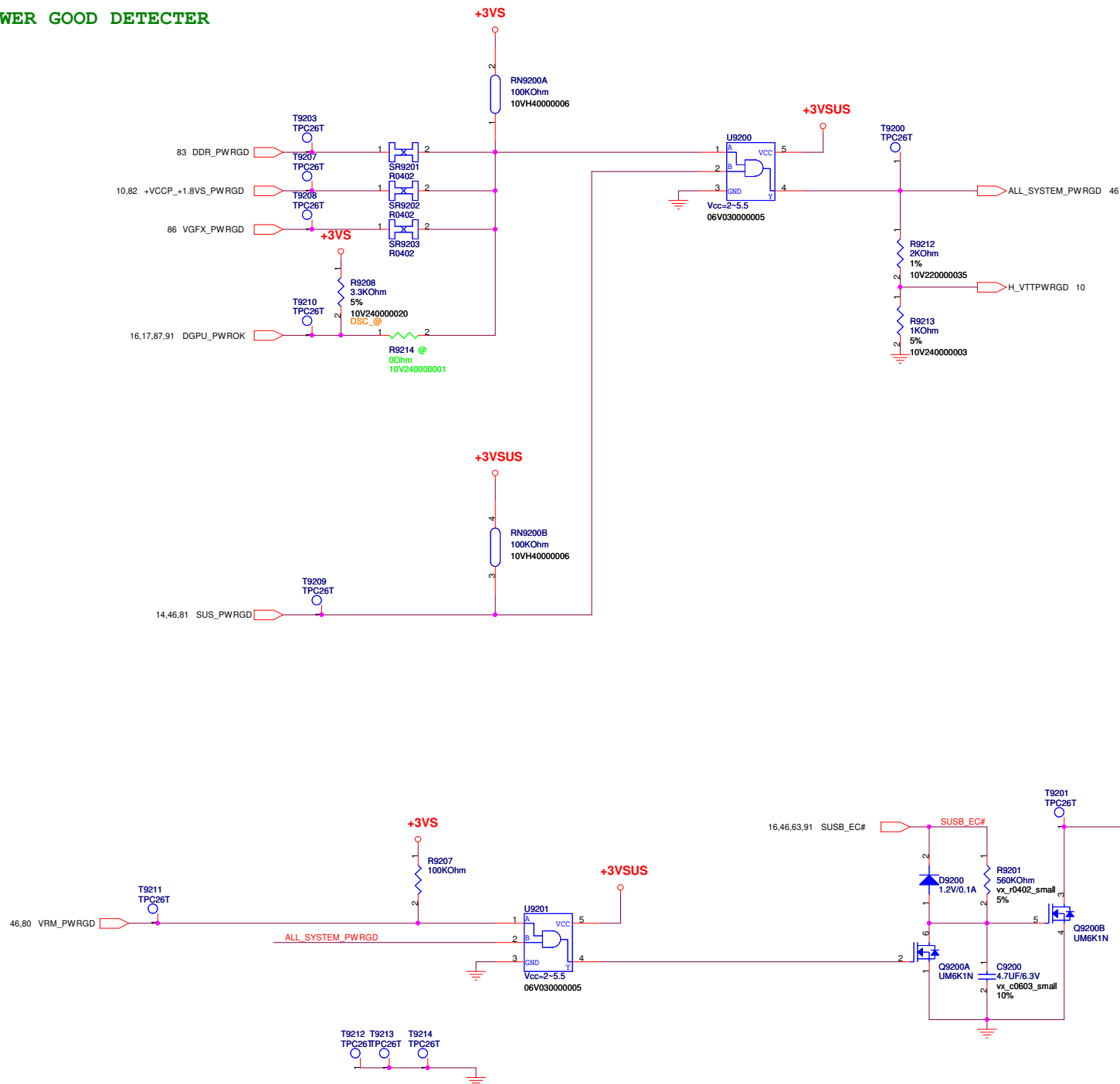
PEGATRON Title :POWER\_LOAD SWITCH

Engineer: Adams\_Lin

Size Custom Project Name AIC70 Rev 1.0

Date: Wednesday, May 04, 2011 Sheet 91 of 77

# POWER GOOD DETECTER



<Variant Name>

PEGATRON		Title :POWER_PROTECT	
Size		Engineer: Adams_Lin	
Custom	Project Name	AIC70	
Date: Wednesday, May 04, 2011	Sheet	92	of 77
		Rev 1.0	

AC\_BAT\_SYS ○ → AC\_BAT\_SYS 37,80,81,82,83,86,87,88  
BAT\_CON ○ → BAT\_CON 63,88  
BAT ○ → BAT 88

+5VA ○ → +5VA 42,49,66,81,88  
+3VA ○ → +3VA 13,18,46,48,63,81

+5VO ○ → +5VO 81,82,83,87,91  
+3VO ○ → +3VO 81,91  
+1.8VO ○ → +1.8VO 82,91  
+1.5VO ○ → +1.5VO 83,91  
+1.05VO ○ → +1.05VO 80,82,86,91  
+VGFX\_CORE\_O ○ → +VGFX\_CORE\_O 86  
+VGA\_VCORE\_O ○ → +VGA\_VCORE\_O 87  
+0.75VO ○ → +0.75VO 83

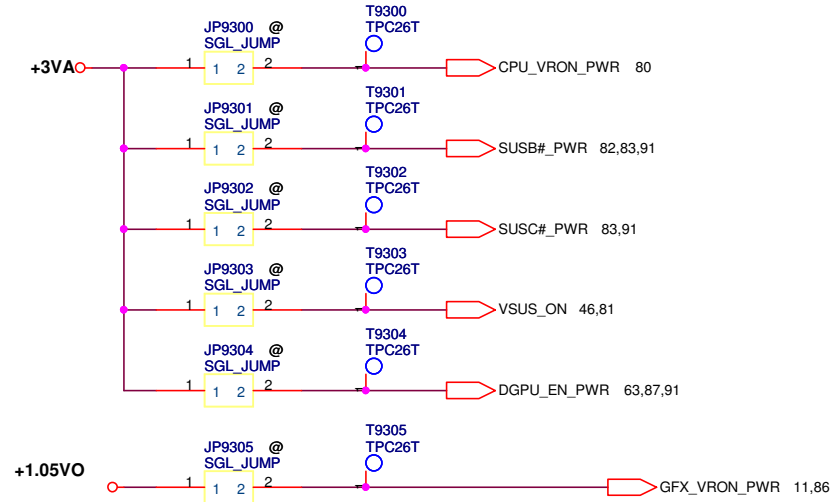
+12VS ○ → +12VS 38,39,91  
+5VS ○ → +5VS 15,19,38,39,41,42,46,48,49,60,63,80,86,91  
+3VS ○ → +3VS 10,13,14,15,16,17,18,19,21,22,24,33,37,38,39,41,46,47,49,60,63,65,80,86,91,92  
+1.8VS ○ → +1.8VS 11,18,19,82  
+1.5VS ○ → +1.5VS 10,11,24,55,63,91  
+0.75VS ○ → +0.75VS 21,22,63,83

+12VSUS ○ → +12VSUS 60,81,91  
+5VSUS ○ → +5VSUS 19,60,61,66,81,91  
+3VSUS ○ → +3VSUS 10,13,14,15,16,17,18,19,33,46,55,81,92

+12V ○ → +12V 91  
+5V ○ → +5V 42,63,91  
+3V ○ → +3V 37,50,63,65,82,91  
+1.5V ○ → +1.5V 10,11,21,22,63,83

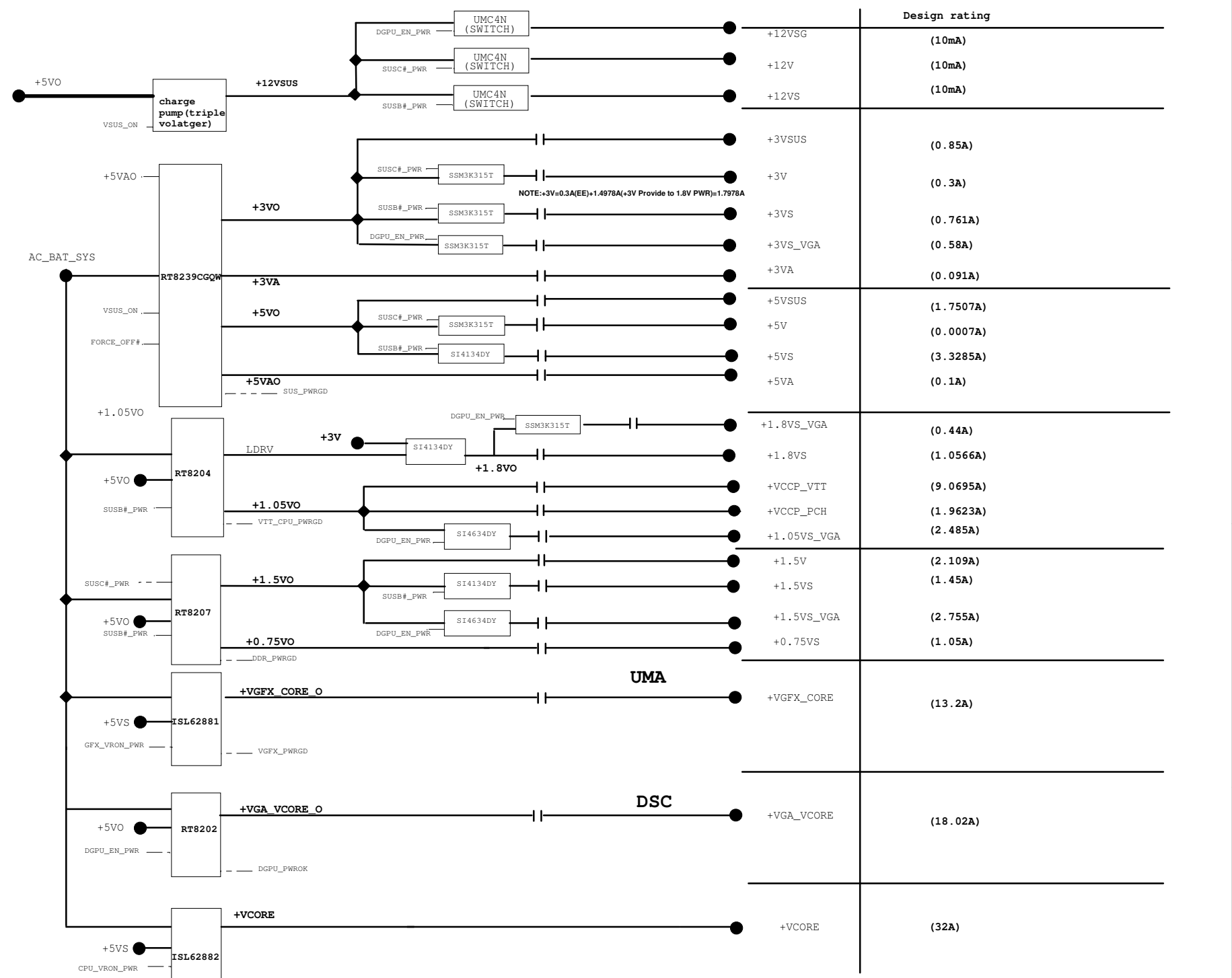
+VGA\_VCORE ○ → +VGA\_VCORE 63,75,87  
+VGFX\_CORE ○ → +VGFX\_CORE 11,86  
+VCORE ○ → +VCORE 11,12,80  
+12VSG ○ → +12VSG 91  
+3VS\_VGA ○ → +3VS\_VGA 70,72,74,91  
+1.8VS\_VGA ○ → +1.8VS\_VGA 63,91  
+1.5VS\_VGA ○ → +1.5VS\_VGA 63,71,76,91  
+1.05VS\_VGA ○ → +1.05VS\_VGA 63,70,71,72,91

## FOR POWER TEST



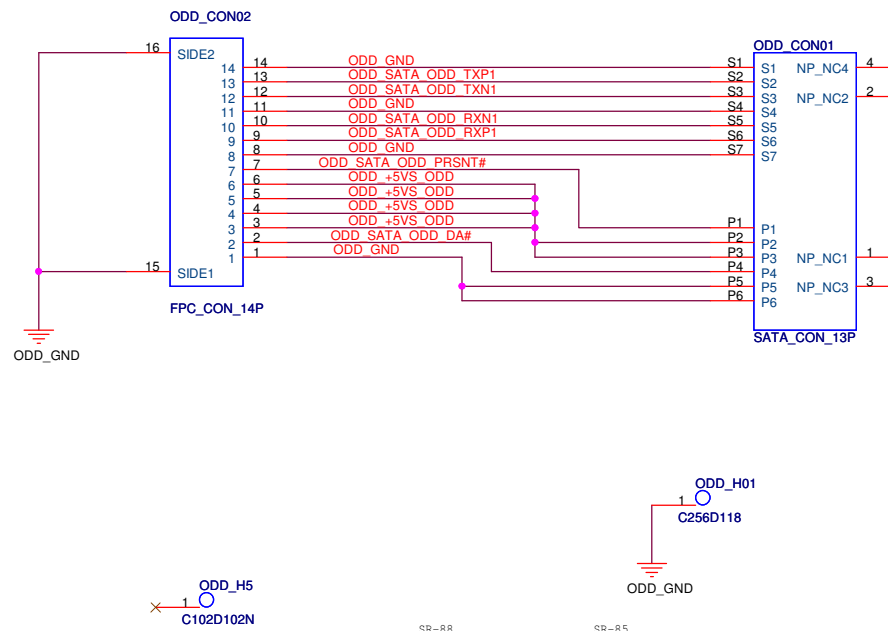
<Variant Name>

<b>PEGATRON</b>		Title : <b>POWER_SIGNAL</b>	
		Engineer: <b>Adams_Lin</b>	
Size Custom	Project Name <b>AIC70</b>		Rev 1.0
Date: <b>Wednesday, May 04, 2011</b>		Sheet	93 of 77



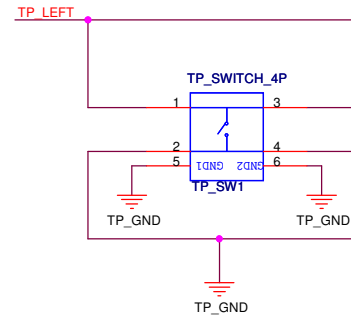
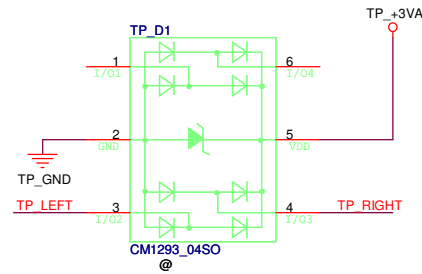
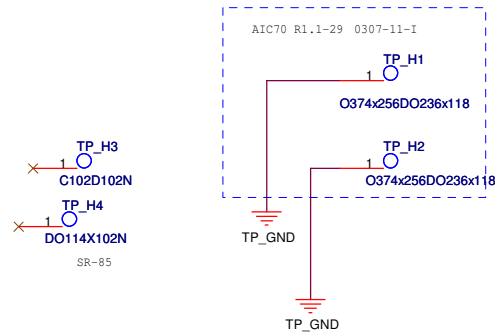


modify notice			modify notice			modify notice		
Item	Date	Description	Item	Date	Description	Item	Date	Description
SR-1	0120-11	P61, A0410, change USB power switch circuit	SR-71	0128-11	P15, Add C1510 (22pF) for Clock fine-tune	AC170	R1-17 0304-11-1	P99, Add 10C7,10C7
SR-2	0120-11	Del P67, P68, Add P33, P34 for LAN	SR-72	0128-11	P33, change R3325, R3331 (4.7k ohm)	AC170	R1-18 0304-11-1	P34, Delete C346
SR-3	0120-11	P48, change KB CN4801	SR-73	0128-11	P39, Un-mount R3907 (HDMI)	AC170	R1-19 0304-11-1	P60, Add SP602 and use /RSD_CABLE option for HDD cable
SR-4	0120-11	P44, change R145 CN4801	SR-74	0128-11	Change connector by list of 0128-11	AC170	R1-20 0304-11-1	P33, Change R371 to 10k pull down for disable OC mode and nstuff C303
SR-5	0120-11	P63, change BATT, con. circuit	SR-75	0129-11	Change HDD COM601 (1224-0010000)	AC170	R1-21 0304-11-1	P60, Delete /17* option
SR-6	0120-11	P65, A02 change PWR LED COM503 circuit	SR-76	0129-11	P97 (A02), Change R024 6 Pad (PWR_001)	AC170	R1-22 0304-11-1	P37, Add PCB ID define
SR-7	0120-11	P60, change HDD COM601	SR-77	0129-11	P41-P50 Change VP part	AC170	R1-23 0304-11-1	P48, Modify TP button optional description
SR-8	0121-11	P44, P45 Del Entry audio circuit (Full)	SR-78	0129-11	P55, Add Q5510, R5515 for BT PCI-E wake up event	AC170	R1-24 0304-11-1	P41, Modify speaker optional description and related net name
SR-9	0121-11	P50, Del Entry speaker circuit	SR-79	0130-11	P50, change footprint for US001 Card reader controller	AC170	R1-25 0307-11-1	P1-P99, Midify schematic optional
SR-10	0121-11	P77, Del B channel VMM * 4 circuit	SR-80	0130-11	P66, change CPU04, GPU2, System screw hole*10	AC170	R1-26 0307-11-1	P18, Add R1824 for PCW SPV *30A power
SR-11	0121-11	P46, Add EC GPIO105 DGPU_PWR_EN for Power	SR-81	0130-11	P46, change RN4601C (RN9202)	AC170	R1-26 0307-11-1	P46, delete R4627,R4625,R4621,R4622,R4615,R4616,R4617,C4609,C4602
SR-12	0121-11	P34, P35, Modify LAN AR8158 (Full)	SR-82	0130-11	P66, change F screw hole *2	AC170	R1-27 0307-11-1	P60, Add R5109,R5110,R5111,R5112
SR-13	0123-11	P61, change DC con. as VP part	SR-83	0130-11	P46, change SHORT PIN (R4601,R4602)	AC170	R1-28 0307-11-1	P66, Delete H6338, change H6337,H6633,H6632
SR-14	0123-11	P60, Change HDD COM601	SR-84	0130-11	P46, P65, change EC GPIO101 (PWR_AMBER_LED) for PWR Brd.	AC170	R1-29 0307-11-1	P88, Change TP_R1,TP_R2
SR-15	0123-11	P7-P37 Change VP part	SR-85	0130-11	Modify Sub board screw hole	AC170	R1-30 0308-11-1	P99, Change 10C8
SR-16	0124-11	P41 Del Entry speaker R4117-R4120	SR-86	0130-11	P34, Change R145 CN03401 1223-00B7000	AC170	R1-31 0308-11-1	P61, Reserve U6105 for reducing connection Loss
SR-17	0124-11	P38-P39 Change VP part	SR-87	0131-11	P74, Change Q7401B(Q9203B)	AC170	R1-31 0308-11-1	P61,Change COM102 to 24 pin (1218-00Q2000)
SR-18	0124-11	P66 Remove LED circuit	SR-88	0131-11	P96, P99, Del Screw hole ODD_R02, change I0H3	AC170	R1-32 0308-11-1	P99, Change 10C805 to 24 pin (1218-00Q2000)
SR-19	0124-11	P48, Reverse KB CN4801	SR-89	0131-11	P97, Change Power Board LED_PWR_LED01	AC170	R1-32 0308-11-1	P46, Mirror vertically Q4501
SR-20	0124-11	P71, Remove GPU Channel B dummy NET	SR-90	0131-11	P60, Change 15" ODD COM505 as VP	AC170	R1-33 0308-11-1	P63, Mirror vertically J6301
SR-21	0124-11	P16, P61, Remove USB_A (HDMI)	SR-91	0131-11	P96-P99, Copy from AAR70 (sub board)	AC170	R1-34 0309-11-1	P80-P94, Merge power schematic AC170_R1_20110310082200.DSN
SR-22	0124-11	P48, Remove TP button circuit				AC170	R1-35 0309-11-1	P98, Add TP022
SR-23	0124-11	P13, Remove Entry A2 R1318, R1346, R1347, R1348, R1349				AC170	R1-36 0309-11-1	P48, Link C4802 Pin1 to COM804 pin1
SR-24	0124-11	P50, Modify COM502 SD socket circuit				AC170	R1-36 0309-11-1	P34, LAN swap on U3403
SR-25	0124-11	P48, Change KB CN4801 PIN definition				AC170	R1-37 0309-11-1	P50, Add SP502 for COM502 pin12 connecting to GND
SR-26	0124-11	P16, P61, change USB power switch circuit				AC170	R1-38 0311-11-1	P46, Change W12_ID
SR-27	0124-11	P41, P46, ALCT21-SPKX_EC_ICH_LED				AC170	R1-39 0311-11-1	P37, Change W12_ID
SR-28	0124-11	P46, P65, Modify LED circuit and EC GPIO definition				AC170	R1-39 0311-11-1	P33, Stuff C3303
SR-29	0125-11	P33 Remove LAN LED circuit				AC170	R1-40 0311-11-1	P80-P94, Update power circuit AC170_R1_2011

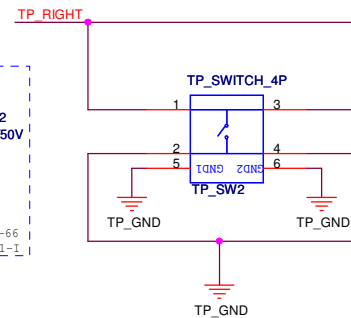
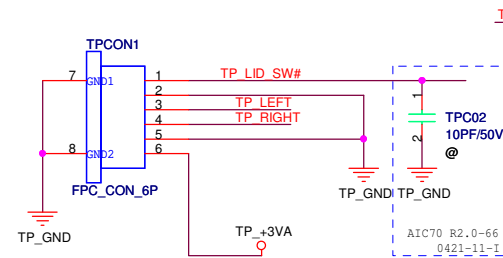
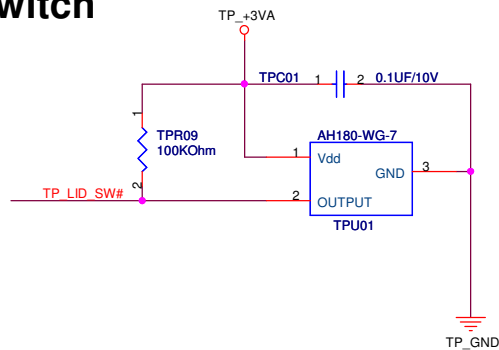


<b>PEGATRON</b> Title : <b>ODD</b>		
BU1-RD Div.1-HW RD Dept.1 Engineer: <b>Johnson Huang</b>		
Size <b>B</b>	Project Name <b>TOD ODD BOARD</b>	Rev <b>2.0</b>
Date: <b>Wednesday, May 04, 2011</b> Sheet <b>96</b> of <b>77</b>		





## LID Switch



AIC70 R2.0-48 0330-11-I  
AIC70 R2.0-67 0421-11-I

<b>PEGATRON</b>		Title : <b>A03 TP</b>	
<OrgName>		Engineer: <b>Johnson Huang</b>	
Size <b>B</b>	Project Name <b>AIH70</b>		Rev <b>1.0</b>
Date: <b>Wednesday, May 04, 2011</b>		Sheet <b>98</b> of <b>99</b>	

